SEPTEMBER 2018

I-Connect007

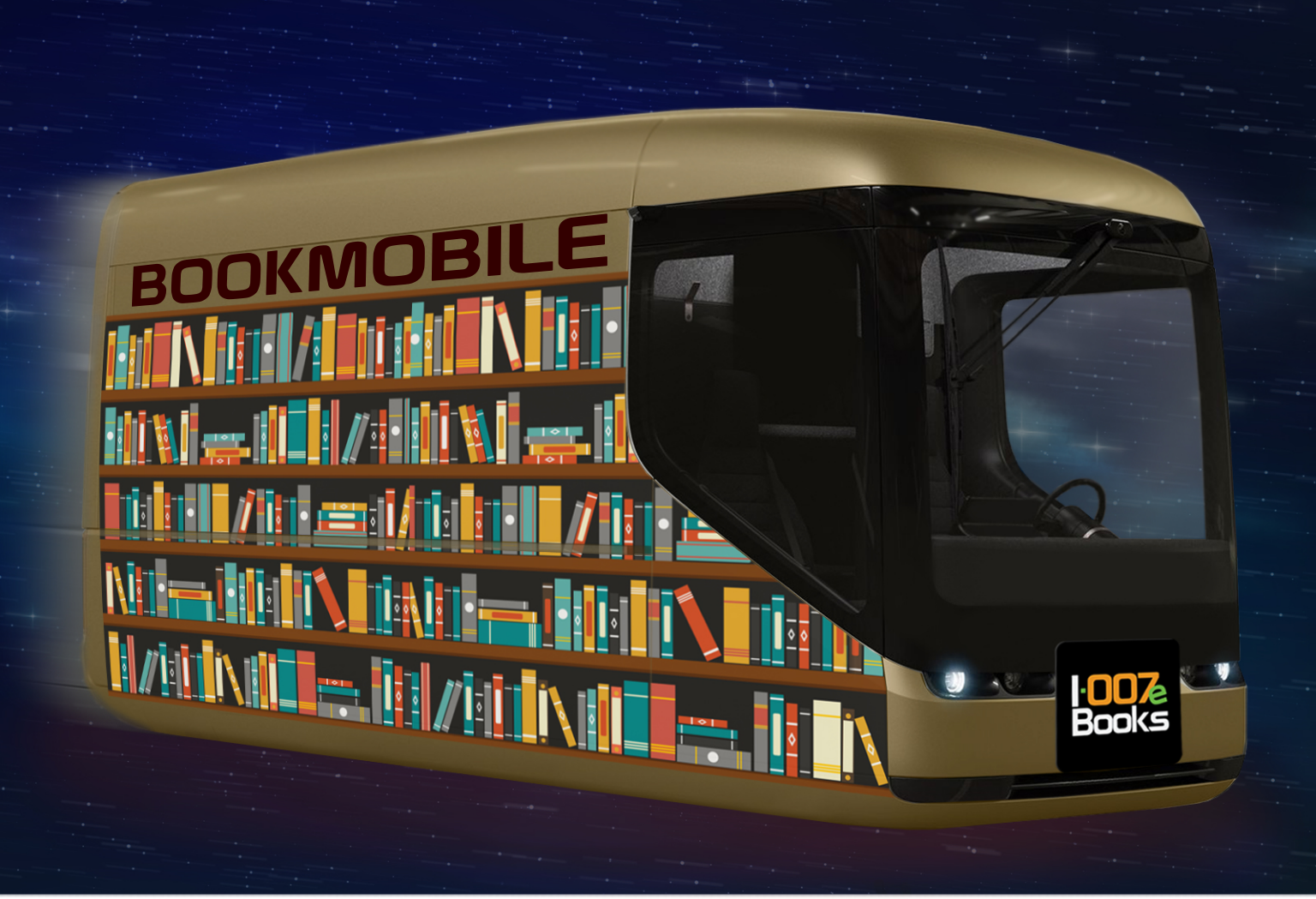
PCB007 MAGAZINE

Get heat relief with low-temperature soldering!

I-007e Books

I-007eBooks.com

Download Now!



Our library is the bookmobile for the 21st century.

Registered members of **my I-Connect007** have access to our ever-growing library of eBooks, which now includes a wide range of topics from DFM to thermal management.

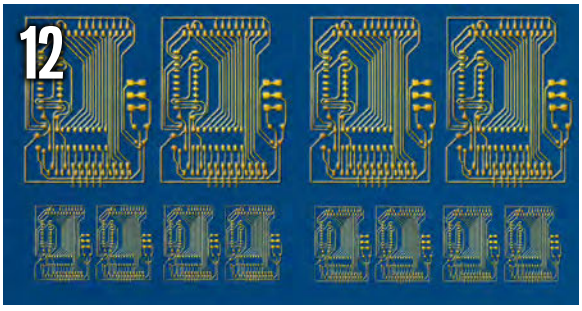
Instead of waiting for the bookmobile, though, our users download new titles with the click of a mouse. It's pretty awesome!

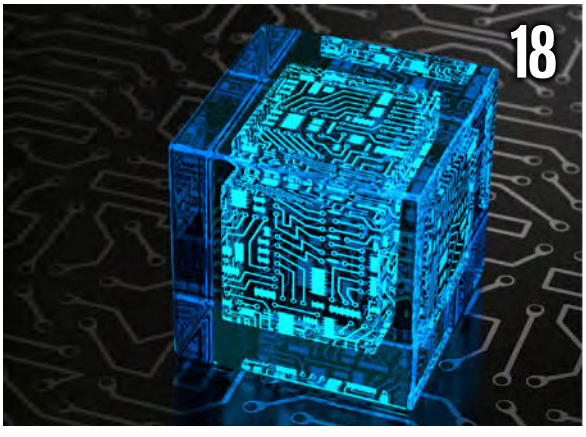
View our eBook library

my I-Connect007
GOOD FOR THE INDUSTRY

I-007e Books

PCB007 MAGAZINE



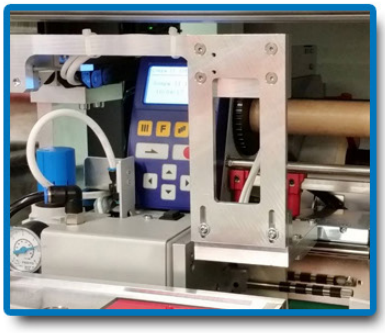


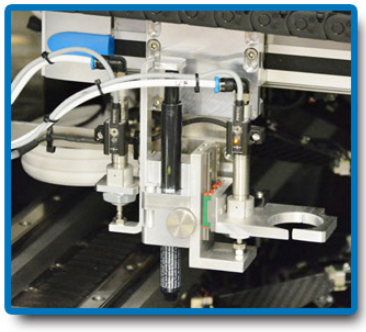
mSAP and SLP

PCBs are now approaching semiconductors with regard to feature sizes. Given this growing trend that shows no signs of slowing down, our experts this month explain substrate-like PCBs (SLP) and the semi-additive processes (SAP) that will help the industry achieve the seemingly impossible (less than 25-micron) features that are coming our way!

Unrivaled Test Speed with Full Automation

Introducing the newly designed atg A8a with 8 test probes and a new high speed “lights out” automation for unrivaled throughput.





Highlights:

- Small footprint (6 square meters)
- Dual shuttle pick & place automation
- High accuracy combined with high test speed
- Pen or label marking option

Watch video

Get more info

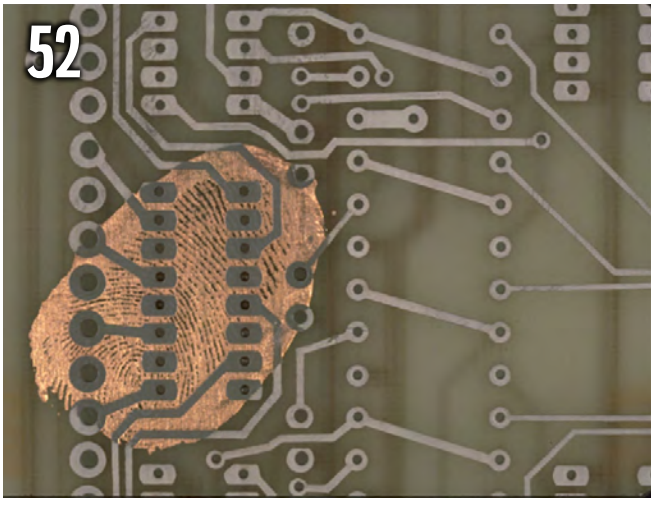
atg

LUTHER & MAELZER

an Xcerra company

atg Luther & Maelzer GmbH
Zum Schlag 3 • 97877 Wertheim • Germany
Phone +49-9342-291-0 • Fax +49-9342-395 10
sales@atg-lm.com • www.atg-lm.com

PCB007 MAGAZINE

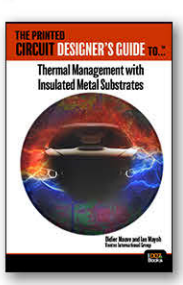


Flexible, reliable Supply Chain Solutions

high quality copper clad laminates & prepreg bonding materials

ventec
INTERNATIONAL GROUP
騰輝電子

Ventec International Group is a world leader in the production of high quality and high performance copper clad laminates and prepregs, with full R&D and product development capabilities. Our global distribution means we can readily supply our products to all markets in all geographic areas.



Get your free copy of *The Printed Circuit Designer's Guide to...Thermal Management with Insulated Metal Substrates.*

DOWNLOAD NOW

PCB WEST 2018
Conference & Exhibition
Connecting Design to Fab to Assembly

Booth 512

Ventec International Group
179 Ward Hill Ave,
Ward Hill, MA 01835,
United States
T: 978-521-9700
E: ordersCA@ventec-usa.com
Follow @VentecLaminates

www.**venteclaminates**.com

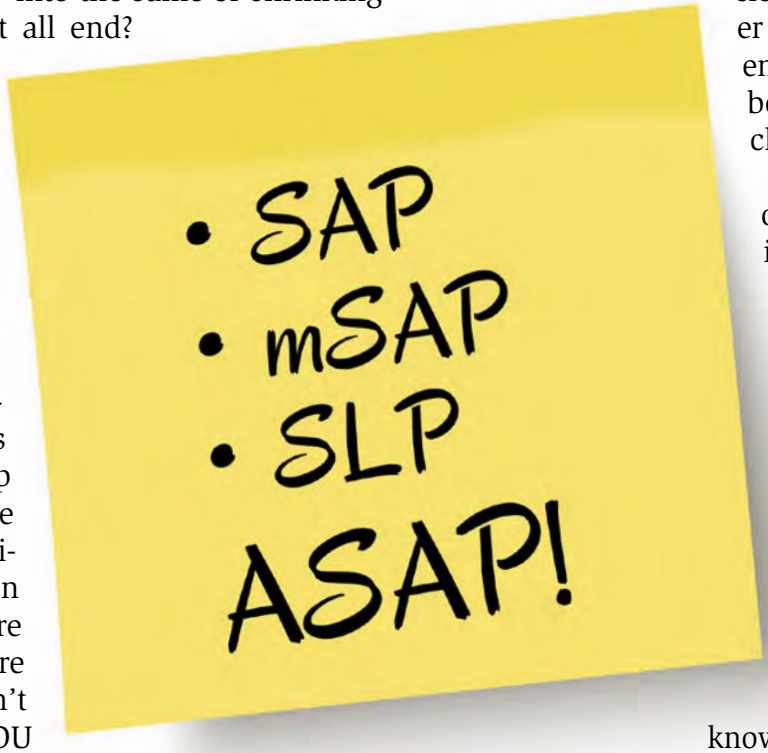
Ventec - wherever technology takes you, we deliver

SLP: The Next Level of Technology

Patty's Perspective
by Patty Goldman, I-CONNECT007

As our electronic devices and machines become more powerful and as Moore's Law chugs along, things in the world of PCBs keep getting smaller. You know the drill—finer lines and spaces, thinner laminates, more layers—cram more circuitry into the same or shrinking area. Where will it all end? Or will it?

PCBs are now approaching semiconductors with regard to feature sizes, which leads us to our topic this month: substrate-like PCBs (SLP) and the semi-additive processes (SAP) that will help us to achieve the seemingly impossible sub-25-micron features that are coming our way. Are you ready? (I can't hear you…ARE YOU READY?)



To help you along that path, our content begins this month with an excellent introduction to the subject by Tara Dunn, Omni PCB, who deals with this technology on a regular basis. She clearly explains the terminology and the process, step by step.

Atotech's Roger Massey goes into greater depth on the market trends and drivers behind the evolution to SLP. He follows this with a close look at the newer PCB technology that enables this, including both equipment and chemistry.

To keep you abreast of what's going on in this segment, Dan Beaulieu interviewed James Rathburn, CEO of HSIO Technologies, which is bridging the gap from IC to PCB using liquid crystal polymer technology. HSIO has partnered with an EMS provider to bring their technology to the market. You need to know about this company.

Elsewhere in this issue, Yole Développement's Emilie Jolivet provides useful market information as you consider how SLP fits with your company's roadmap. First reviewing the evolution of PCBs in smartphones to present day

pluritec

Celebrating 50 Years of Service!

50

1968-2018

The Pluritec brands that provide you with tomorrow's technology today !

pluritec

X-ray Optimizer &
Automated flash/Bevel/Corner
rounding panel prep

Drills & Routers
24/7 automation

MORE INFO

ECOspray SYSTEM

Multi-color solder mask
coaters with 15 minute
fast tack oven

MORE INFO

IS INTERNATIONAL SUPPLIES

Wet Process
developers - etchers - strippers
Cobra - MEC Etch
Shadow - ChemClean

Mechanical prep
Debur - Scubbers - Pumice/Oxide
PCB brush & Chemical washing

MORE INFO

www.pluritec.com | info@pluritec.com

use of SLP technology, Jolivet then projects use in a wide variety of markets.

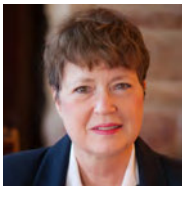
For those of you out there in the trenches, we have another good troubleshooting column by RBP's Mike Carano, this time on resist lock-in and extraneous copper. As always, Mike provides both cause and action to get you through this problem.

Next, we have an interesting article on copper pillar plating systems. Copper pillars are useful for removing heat from components, but they are not particularly easy to create. MacDermid Enthone's Albert Angstenberger explains both theory and practice for these, as well as delves into via fill and through-hole plating as they relate to the pillar plating.

Bringing up the rear is Steve Williams, The Right Approach Consulting, with a discussion on global sourcing. Whether or not you are involved in choosing PCB suppliers, this article outlines "5 Cs" that truly can apply to any supplier-partner relationship—regardless of which side you are on.

Lastly, IPC's John Mitchell introduces us to Nicolas Robin, IPC's new senior director in Europe. Robin will represent IPC's public policy in Europe, with additional membership-related responsibilities.

Well, folks, this is my last hurrah as managing editor of *PCB007 Magazine.* As I transition to a lighter schedule, Nolan Johnson will be at the helm now. Don't miss his debut in next month's issue that focuses on the automated factory. Not to worry, I won't disappear—at least not yet. I will be managing our quarterly tome, *Flex007 Magazine,* which next appears in late October. Keep your eye out for that—which will be a lot easier if you subscribe. Aren't you going to miss my nagging? **PCB007**



Patricia Goldman is managing editor of *PCB007 Magazine.* To contact Goldman, click here.

Tags that Turn Everyday Objects into Smart, Connected Devices

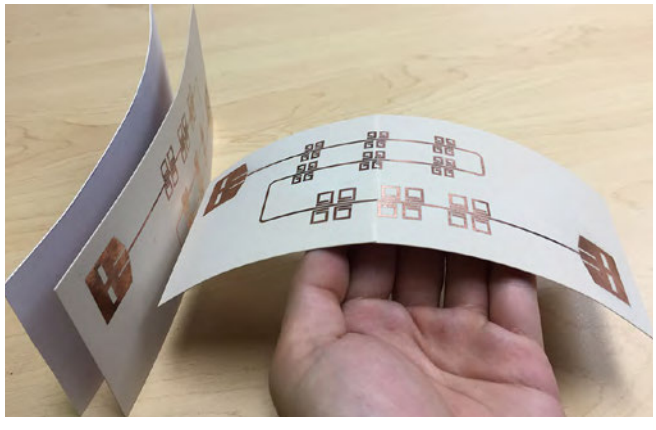
Engineers have developed printable metal tags that could be attached to everyday objects and turn them into smart Internet of Things devices.

The metal tags are made from patterns of copper foil printed onto thin, flexible, paper-like substrates made to reflect Wi-Fi signals. The tags work like mirrors that reflect radio signals from a Wi-Fi router. When a user's finger touches these mirrors, it disturbs the reflected Wi-Fi signals in such a way that can be remotely sensed by a Wi-Fi receiver, like a smartphone.

The tags can be tacked onto plain objects that people touch and interact with every day, like water bottles, walls or doors. These plain objects then essentially become smart, connected devices that can signal a Wi-Fi device whenever a user interacts with them. The tags can also be fashioned into thin keypads or smart home control panels that can be used to remotely operate Wi-Fi-connected speakers, smart lights and other Internet of Things appliances.

"Our vision is to expand the Internet of Things to go beyond just connecting smartphones, smartwatches and other high-end devices," said senior author Xinyu Zhang, a professor of electrical and computer engineering at the UC San Diego Jacobs School of Engineering and member of the Center for Wireless Communications at UC San Diego. "We're developing low-cost, battery-free, chipless, printable sensors that can include everyday objects as part of the Internet of Things."

(Source: UC San Diego)



Printed thin, flexible LiveTag tags in comparison with a piece of photo paper (far left). Photos courtesy of Xinyu Zhang

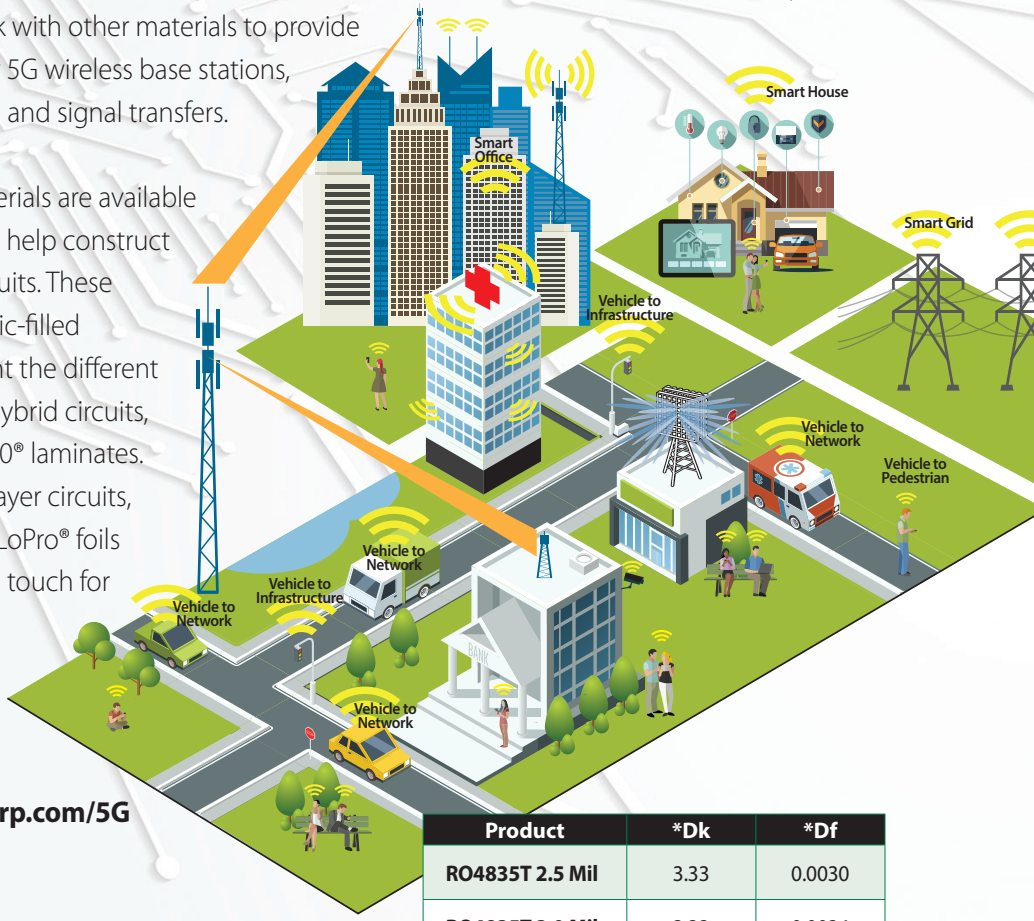
5G: Higher Frequencies!

Do you have the **right** circuit materials?

Frequencies at 28 GHz and higher will soon be used in Fifth Generation (5G) wireless communications networks. 5G infrastructure will depend on low-loss circuit materials engineered for high frequencies, materials such as RO4835T™ laminates and RO4450T™ bonding materials from Rogers Corporation!

Rogers RO4835T spread-glass-reinforced, ceramic-filled laminates are low-loss materials in 2.5, 3.0, and 4.0 mil thicknesses. They are well suited for millimeter-wave frequencies as part of the inner cores of 5G hybrid multilayer PCBs. They can work with other materials to provide the many functions needed by 5G wireless base stations, including power, signal control and signal transfers.

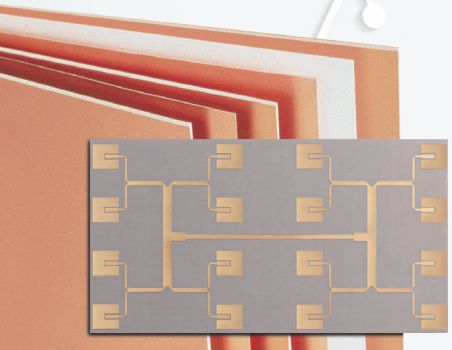
Rogers RO4450T bonding materials are available in 3, 4, and 5 mil thicknesses to help construct those 5G hybrid multilayer circuits. These spread-glass-reinforced, ceramic-filled bonding materials complement the different materials that will form these hybrid circuits, including RO4835T and RO4000® laminates. And for many 5G hybrid multilayer circuits, Rogers CU4000™ and CU4000 LoPro® foils will provide a suitable finishing touch for many hybrid multilayer circuit foil lamination designs.



5G is coming! Do you have the right circuit materials?
Learn more at **www.rogerscorp.com/5G**

Product	*Dk	*Df
RO4835T 2.5 Mil	3.33	0.0030
RO4835T 3.0 Mil	3.33	0.0034
RO4835T 4.0 Mil	3.32	0.0036
RO4450T 3.0 Mil	3.23	0.0039
RO4450T 4.0 Mil	3.35	0.0040
RO4450T 5.0 Mil	3.28	0.0038

** IPC TM-650 2.5.5.5 Clamped Stripline at 10 GHz - 23°C*

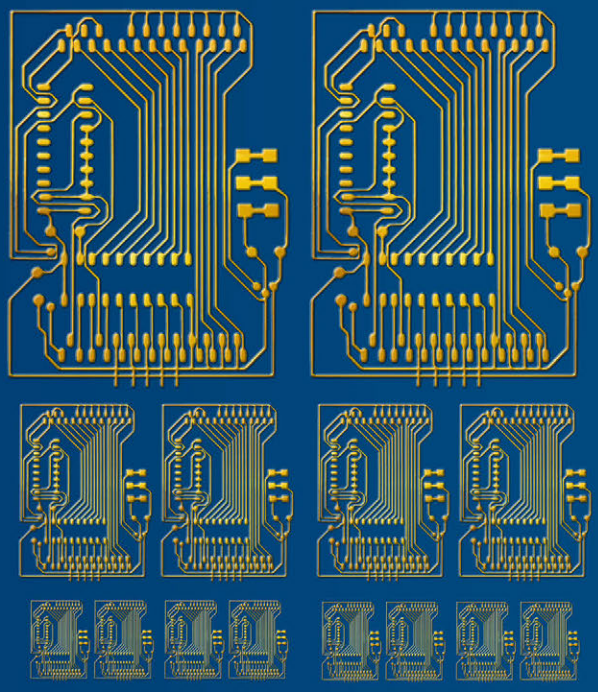


ROGERS CORPORATION
Advanced Connectivity Solutions

USA - AZ, tel. +1 480-961-1382 • EUROPE - BELGIUM, tel. +32 9 235 3611
www.rogerscorp.com

Additive Electronics:

PCB Scale to IC Scale



Feature by Tara Dunn
OMNI PCB

SAP, mSAP, SLP—what kind of crazy acronyms have we adopted now, and how much do you really need to know? In terms of consumer electronics, there is a good chance that the smartphone attached to your hand at all times contains a PCB fabricated with this technology—or at the very least, the next-generation smartphone that you purchase will utilize mSAP technology. In terms of current-day PCB design and fabrication, that really depends on where you are now with technology.

The standard subtractive-etch process serves the industry well. Developments in materials, chemistry and equipment enable the traditional PCB fabrication process to achieve feature sizes such as line and space down to 30 microns. Larger shops with more sophisticated capabilities are building this technology today. Mainstream PCB manufacturing is often limited to 50-75 microns (μm) line and space. But the electronics industry is evolving quickly. Propelled by the demand for more sophisticated electronics, the PCB design is being tasked with finer lines, thinner materials and smaller via sizes. A traditional progression is to first move to HDI technology with microvias and multiple lamination cycles for fabrication. Today's mSAP and SAP technology offers an advanced approach, with line and space capabilities of less than 25 microns, to meet these exceedingly complex design requirements.

A Few Definitions

- Subtractive etch process: commonly used to fabricate printed circuit boards. This process begins with copper-clad laminate, which is masked and etched (copper is subtracted) to form traces
- Additive PCB fabrication: this process utilizes additive process steps, rather than subtractive process steps to form traces
- SAP: semi-additive process, adopted from IC fabrication practices
- mSAP: modified semi-additive process, adopted from IC fabrication practices
- SLP: substrate-like PCB; a PCB using mSAP or SAP technology instead of subtractive etch technology

Innovation: It's What Leaders Do.

What's next from the leader in flex PCB processing?

UP NEXT:
New leading-edge laser technology and extended control capabilities. Optimized to provide unmatched value for even the latest applications challenges.

COMING SOON:
New innovative solution for HDI PCB manufacturing and IC Packaging.

- Optimized laser capabilities to improve performance for key applications
- Advanced beam positioning to increase throughput
- Extended laser control to deliver higher yield and productivity
- New technology to enhance system robustness
- Combination of high quality and high throughput to lower your total cost of ownership

Focus on Possibilities, Not Limitations.

esi®

Designed for Brilliance.
Engineered for Production.

See ESI's Current Lineup of PCB Processing Solutions

www.esi.com

SAP and mSAP are processes commonly used in IC substrate fabrication. As this technology is adapted to and integrated into PCB manufacturing it has the potential to fill a gap between IC fabrication and PCB fabrication capabilities. Subtractive etch PCB fabrication has a limiting factor of finer line/space capability and IC fabrication is limited by a small overall panel size. As these processes are adapted to PCB manufacturing, there is the opportunity to fabricate on larger panel sizes with sub-25-micron trace and space.

In PCB manufacturing, both SAP and mSAP processing start with the core dielectric and a thin layer of copper.

In PCB manufacturing, both SAP and mSAP processing start with the core dielectric and a thin layer of copper. A common differentiation between the two processes is the thickness of the seed copper layer. Generally, SAP processing begins with a thin electroless copper coating (less than 1.5 µm) and mSAP begins with a thin laminated copper foil (greater than 1.5 µm). There are multiple ways to approach this technology and decisions can be based on volume requirements, costs, capital investment needed and process knowledge.

The Process

Both the SAP and mSAP, follow a similar process. First, a thin layer of copper is coated on the substrate. This is followed by a negative pattern design. Copper is then electroplated to the desired thickness and the seed copper layer is removed.

For insight into additive PCB processing steps, I spoke with Mike Vinson, president and CTO of Averatek, a California-based company specializing in a catalytic ink that enables additive processing. He shared information and insight into technology based on Averatek's IP. Averatek's Atomic Layer Deposition (ALD) precursor ink can be utilized for both low-volume and high-volume applications and fully additive or semi-additive processes. The catalytic ink controls the horizontal dimensions of the line width and spacing. The vertical dimension of the metal thickness is controlled by an additive process that deposits metal only on the patterns defined by the photoresist.

Averatek's process consists of six basic steps:

1. Drill vias in the substrate using either mechanical or laser drills. (Note: This step is optional if the customer's process includes creating vias after the Averatek process has been completed or does not include vias.
2. The substrate is then prepared for processing. In most cases, this is a simple cleaning and mounting of the material in the appropriate material handling system.
3. Coat and cure the substrate with the Averatek ALD precursor catalytic ink, resulting in a sub-nano-layer (< 1 nm thick) of catalytic material.
4. Deposit electroless copper on the precursor. The copper thickness ranges from 0.1 µm to 1.0 µm.
5. Image a layer of photoresist using photolithographic techniques to create the patterns where copper will be deposited. The geometry of lines and spaces that can be produced at this point is anything above 5 µm.
6. Electrolytic copper plating will finish out the circuits, followed by stripping the remainder of the resist and flash etching.

This technology enables very fine lines on flexible or rigid substrates, among other materials, at a very competitive cost. Since the holes are plated along with the traces, a smooth and seamless transition can be made. Many of the applications requiring fine-line geometries support high-speed and therefore high-frequency signals, the smoothness and quality of the conducting metal is critical. The process described above produces conductors whose cross-sections are rounded and whose surfaces are

smooth. Both qualities are ideal for high-frequency circuitry to minimize crosstalk, shorts, and energy losses.

Markets Utilizing Additive Fabrication

The smartphone market is the most visible market to bring mSAP processes to high volume production, with Apple leading the pack with the launch of the iPhone 8 and iPhone X in 2017 and other manufacturers quickly adopting the technology. Current designs are blending a combination of layers done with subtractive etch and layers with the mSAP technology. mSAP technology allows for a thinner, smaller motherboard design. This was critical to the design to allow more room for the battery and extended battery life for consumers. The technology in the iPhone X reveals 30-micron trace and space (Figure 1). Predictions for the coming years are for trace and space to be in the 10-micron range.

The concept of blending the layers, utilizing the mSAP process for layers with tight pin-outs and tough routing, and combining with other layers that are processed with subtractive etch, was proven to be effective in the smartphone market and is spreading to other markets: wearables, medical devices, medical implantables, automotive and aerospace and defense. It is hard to deny the advantages of moving from 10-layer HDI with four-lamination-cycles designs, to a 6-layer single- or double-lamination design. But, this does force us to look at both design and fabrication in a new way. As fabricators develop processes for this type of requirement, design rules need to be established and reliability testing needs to be completed.

Figure 1: Motherboard found in the iPhone X. (Source: IFIXIT and Creative Electron)

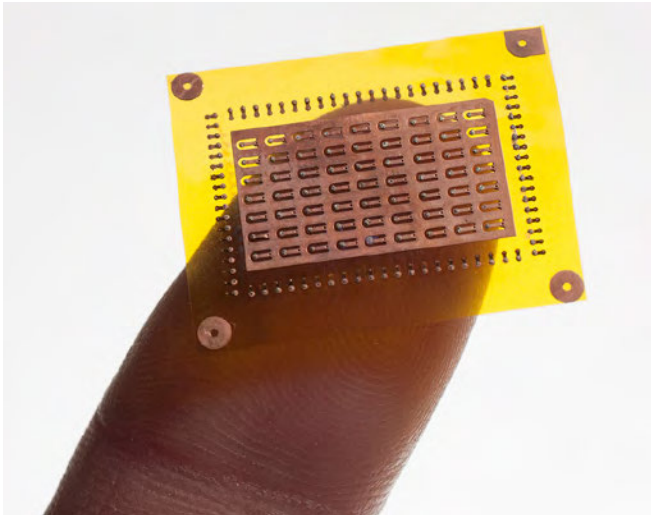


Figure 2: Circuit fabricated with SAP technology. (Source: Averatek)

Real-World Applications

What type of applications are discussing or adopting this new PCB technology? Applications that need extremely thin copper, applications that are concerned with space and weight, and applications that have complex pin-outs pushing the capabilities of traditional PCB manufacturing are all ones that could utilize SAP or mSAP technology.

One example is medical implantables using 20-micron trace and space technology, with a double-sided design, on polyimide, with gold conductors. The combination of polyimide and gold is also compelling for biocompatibility reasons (Figure 2).

Military/aerospace applications with high-density interconnect designs requiring tight pin-outs now have the option of finer lines and smaller vias. Following stack-up structures similar to the work done in the smartphone designs, success is being found domestically by integrating layers with SAP technology and layers with subtractive etch technology, reducing layer count and reducing costly lamination cycles.

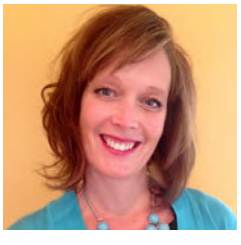
Figure 3: Averatek's ALD provides design opportunities with other materials. (Source: Averatek)

Wearable technology is another forerunner. SAP and mSAP enables thinner, lighter weight, more flexible circuity—all attributes catering to the wearable technology market.

Averatek's ALD ink enables printing circuit patterns directly on rounded or unusually shaped structures, including 3D products, the curved end of a catheter and others that the traditional subtractive etch processes have not been able to serve. This ALD ink has also found success in the emerging e-textiles market. Applying the ALD ink to various fabrics and plating with electroless copper results in conductive material that can then be integrated in e-textiles applications (Figure 3). Both these application areas enable design development in growing markets not traditionally served by PCB fabricators.

Recapping, SAP, mSAP and SLP is a process that is currently serving the highly visible, high-volume, smartphone market. The PCB industry world-wide is taking notice and looking for other opportunities to implement this technology in designs with requirements for thin copper, sub 25-micron line and space and complex HDI designs. This is a new technology pushing fabricators to look at equipment and processes to determine how to adapt from a subtractive process to an additive process. This technology also pushes designers to look at printed circuits in a new way and provides a new tool to solve complex design issues.

I believe pushing us outside of our comfort zone is a good thing, even though it is difficult, and the resulting additional technical capabilities will propel us forward to solve the increasingly sophisticated electronics requirements. Watch for information from SMTA regarding a new conference in 2019, "Additive Electronics: IC Scale to PCB Scale," which intends to address the gap between traditional subtractive etch processing and mSAP and SAP technology. **PCB007**



Tara Dunn is the president of Omni PCB, a manufacturer's rep firm specializing in the printed circuit board industry. To read past columns or to contact Dunn, click here.

Electronics Coatings for the Digital Era

ELECTRA

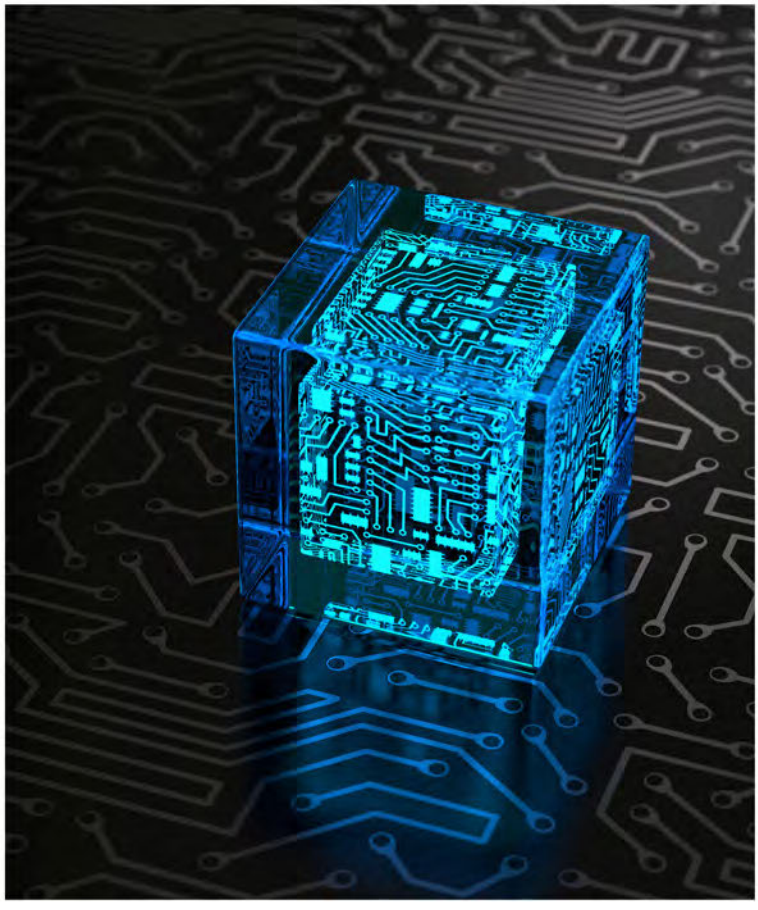
EMP110 Soldermask

- Reputation for reliability
- Meets or exceeds automotive requirements
- Widely used in the automotive industry

RoHS COMPLIANT

T +44 (0)1732 811118
info@electrapolymers.com
www.electrapolymers.com

The Changing Shape of the HDI Market



Feature by Roger Massey
ATOTECH

Evolution of the HDI PCB

Since their advent in the early-to-mid-1990s, high-density interconnect (HDI) PCBs have undergone several changes and could now be said to be entering their third evolution. Based on subtractive, or print-and-etch processes, the early HDI panels made use of traditional cores and sequential lamination steps to produce high-end boards with ~60 µm line and space (L/S) capabilities. But most importantly, they relied on microvias to enable their high interconnect density, which, at that time, could not be readily achieved with other technologies.

As board producers improved their processes, HDI board capability also improved; with the release of what we now accept as the smartphone, in the early 2000s, the second generation of HDI panels came into being. While the laser microvias remained, stacked vias began to replace staggered vias, and in combination with the "any layer" or "every layer" build-up technique, these new HDI boards eventually begin to exhibit 40 µm L/S.

Still based on subtractive technologies, this any-layer approach remains the king of the HDI techniques, and it is true to say that the majority of the advanced HDI PCBs that are typical to mobile devices are still produced with this technique. However, in 2017, the HDI market began its next evolution by starting to move away from subtractive processes and into those based on pattern plating. While still reasonably common in Europe and the USA, in Asia HDI has been generally limited to IC substrate manufacturers.

Semi-additive processing (SAP) uses pattern plating processes to realize features <15 µm, and while this size is needed for package substrates, it's not yet called for in advanced HDI boards. However, mSAP and amSAP are modified and advanced modified variations which are now on track to become the next generation of HDI PCBs.

A new set of rules for PCB production

Less process steps. CAM to etch in minutes instead of hours. Maximum yield. Minimal environmental impact.These are just a few of the PCB production rules that Lunaris has redefined.

We've put together a complete set of all the new rules made possible by Lunaris ...get yours today!

Download all the new rules:
The Official Lunaris Rulebook

CLICK HERE TO DOWNLOAD

mutracx
THE BETTER WAY

www.mutracx.com

Market Trends and Drivers

Handset Design

As is usually the case, the drive for improvements in PCBs usually comes from the market, and with HDI boards this has really meant changes in mobile handset design.

Looking at Figure 1, we can see an evolution of the mobile phone, and several interesting observations appear:

- Handset thickness has steadily reduced and is currently 7-8 mm
- Handset area has increased, with 90-100 cm^2 now being typical
- Battery size has generally increased in proportion with overall handset size
- Primary PCB area has decreased from approx. 25 cm^2 to 15-20 cm^2
- PCB layer count has remained pretty constant at approx. 10 layer
- PCB complexity has increased, L/S reduced from 60 µm to approx. 30 µm

So, in order to allow for modern handset design, while leaving sufficient space for all the other components to fit into the handset case, HDI PCBs had to become thinner, smaller and much more complex!

Die Packaging

Whilst some of the changes in PCB thickness and area demands can be attributed to handset physical design, which has certainly contributed towards increased PCB complexity, much of the additional complexity can be traced to die packaging needs. And, as many components are now packaged in some form of area array, we need to consider solder ball count, diameter and pitch.

In simple terms, die are more complex than ever, and packaged or not, this generally means they have more I/Os than they had in the past. In order to push I/O count, and still minimize package footprint, one general trend is to try and decrease both solder ball diameter and pitch. At the same time, an increase in I/O count also means more traces are required to route those I/Os, and this can usually be achieved through finer lines, assuming the area and layer count restrictions outlined above are to be followed.

Figure 1 shows the most recent handset designs have a minimum L/S requirement of 30 µm, dropping from 50 µm in earlier generations. This cannot be achieved with fully subtractive PCB processes as issues during etch become unacceptable, so there is a need to adopt one of the variations of the SAP process-

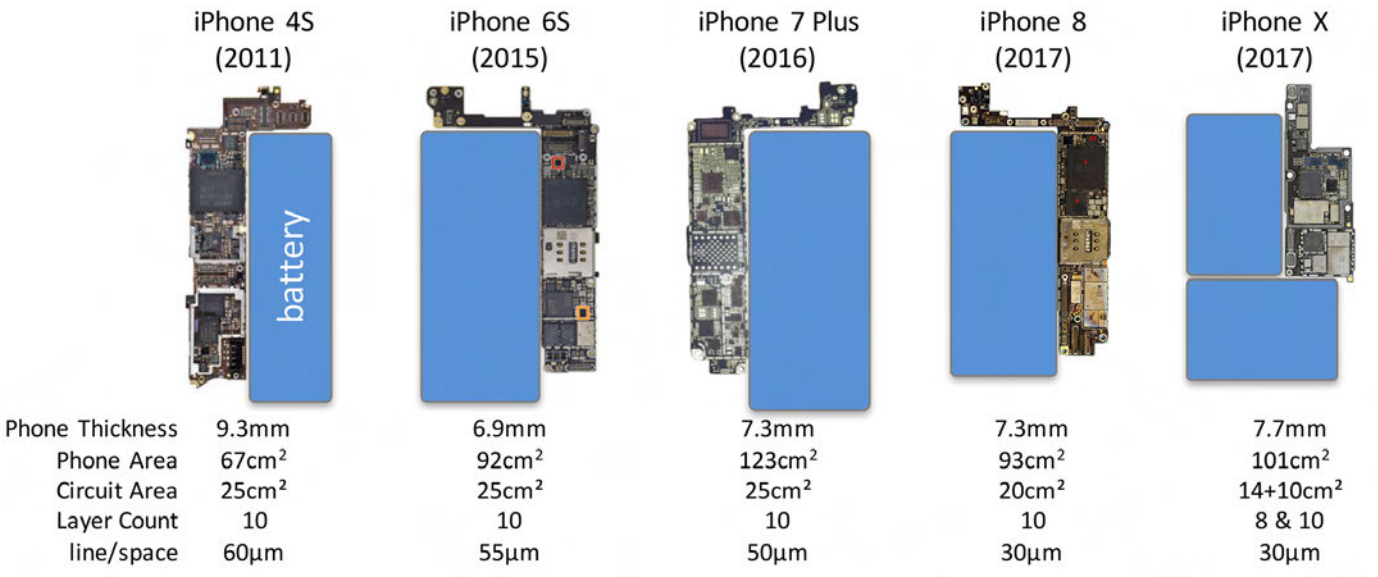


Figure 1: Evolution of the smartphone. (Sources: iFixit, TechInsights, Teardown.com, IHS, Prismark Partners)

Panasonic

For Millimeter-wave Band Antennas
NEW Material replacement of PTFE

Halogen-free
Ultra-low Transmission Loss
Circuit Board Material

R-5515

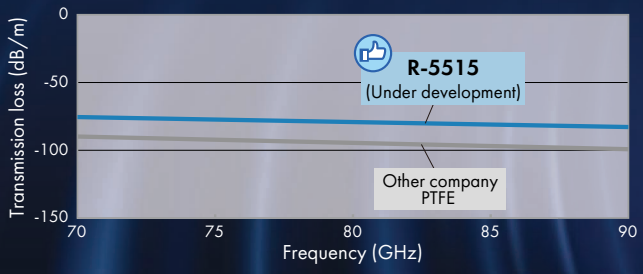
Under Development

Features

- Low transmission loss (Equality or Better than PTFE)
- Dk 3.0 Df 0.0019@10GHz
- Reduce PCB process cost (vs. PTFE)

Transmission Loss

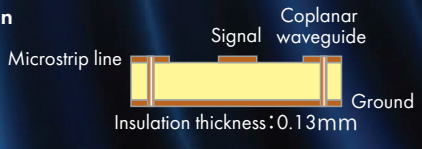
- Frequency dependence by Transmission loss (70-90GHz)



- Transmission loss at 79GHz

Material	Transmission loss (dB/m)	Dk (Design)
R-5515	79	3.22
Other company PTFE	96	3.14

- Construction



Contact us

More information

DISTRIBUTOR IN NORTH AMERICA
MATRIX USA INC.
TORONTO • SANTA ANA • SANTA CLARA • CHICAGO • MINNESOTA
Visit our website at www.matrixusa.us

Partnering to go beyond.

Electronic Materials
Panasonic Corporation

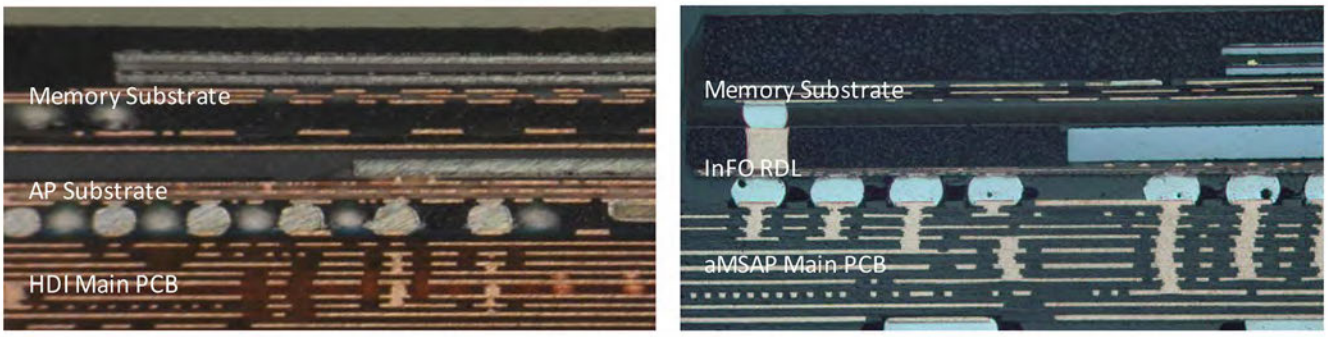


Figure 2: Substrate-based AP package (left); substrate-less AP package using TSMC InFO (right). (Sources: Prismark Partners, left; Atotech, right)

es, which in turn, requires a complete review of the PCB production process.

This recent drive to reduce L/S can be linked to the release of the iPhone 7 in 2016. With the iPhone 7, Apple selected to abandon substrate-based application processor (AP) packages and opted for the new InFO (integrated fanout) package from TSMC.

With InFO, the typical IC substrate is replaced with fine feature redistribution layers (RDL) deposited directly onto the die and package mold surface. Collectively grouped as fan-out wafer level packages (FO-WLP), these package types can offer not only reduced thickness, but allow sub 5 µm L/S to be applied in the RDL, enabling an appreciable increase in I/O count, and with the associated reduction in pad pitch, this can occur without sacrificing real estate; more importantly, all of this is achieved while maximizing electrical and thermal performance which are critical in modern smartphone designs.

PCB Technology Trends

Outside of packaging, there are a number of other trends going on within PCB production, all of which impact critical steps of manufacture, and will affect HDI design going forward.

Using established tool sets, the majority of today's microvias are formed by CO_2 lasers. One negative of the process is appreciable amounts of heat generated within the substrate, which leads to the formation of a heat-affected zone (HAZ) at each drill site, which impacts minimum via pitch as well as their size and quality.

In order to resolve this, laser manufacturers are developing new tools with ultra-short pulse (USP) lasers, which replace the existing nano-

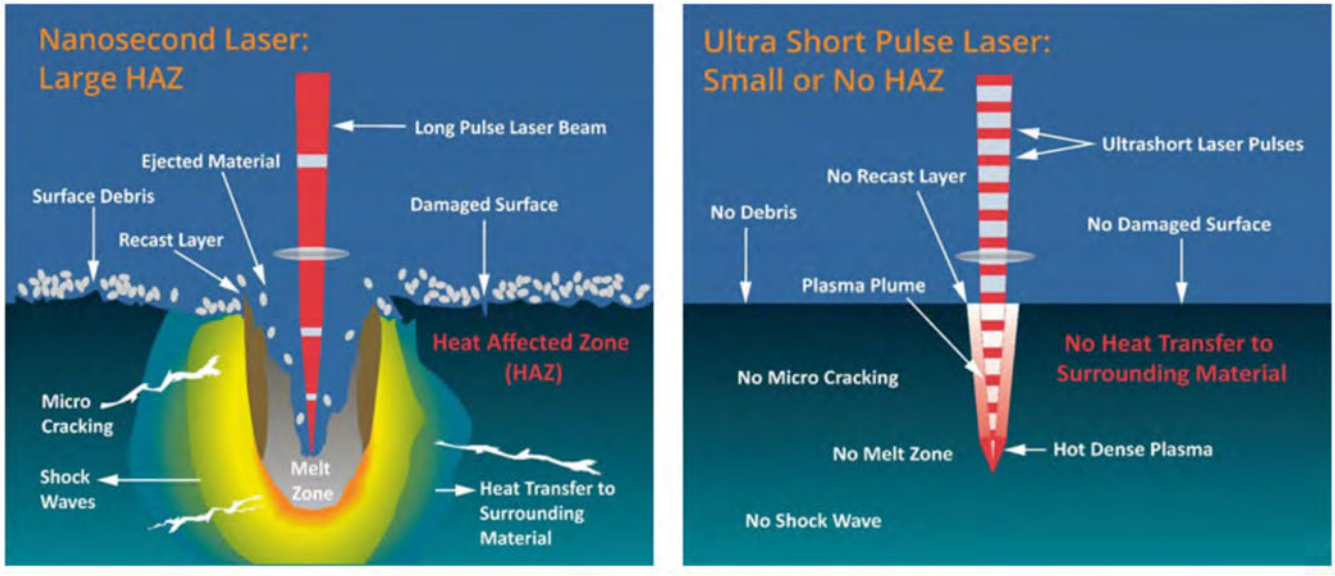


Figure 3: Impact of laser pulse duration on HAZ. (Source: IPG Photonics)

Excellon

Manufacturers of precision Micro-Machining Solutions for over 50 Years

COBRA II

Hybrid laser system

689

6-station precision drilling and routing system

HS-1L DS

Single-station, dual spindle high-speed system

136L

High accuracy and speed

154L

Large panel applications

HS-2L

2-station, high-speed

129

Single-station precision system

Move into the future with the latest innovations in Fabrication Technology from the Industry Leader!

www.excellon.com

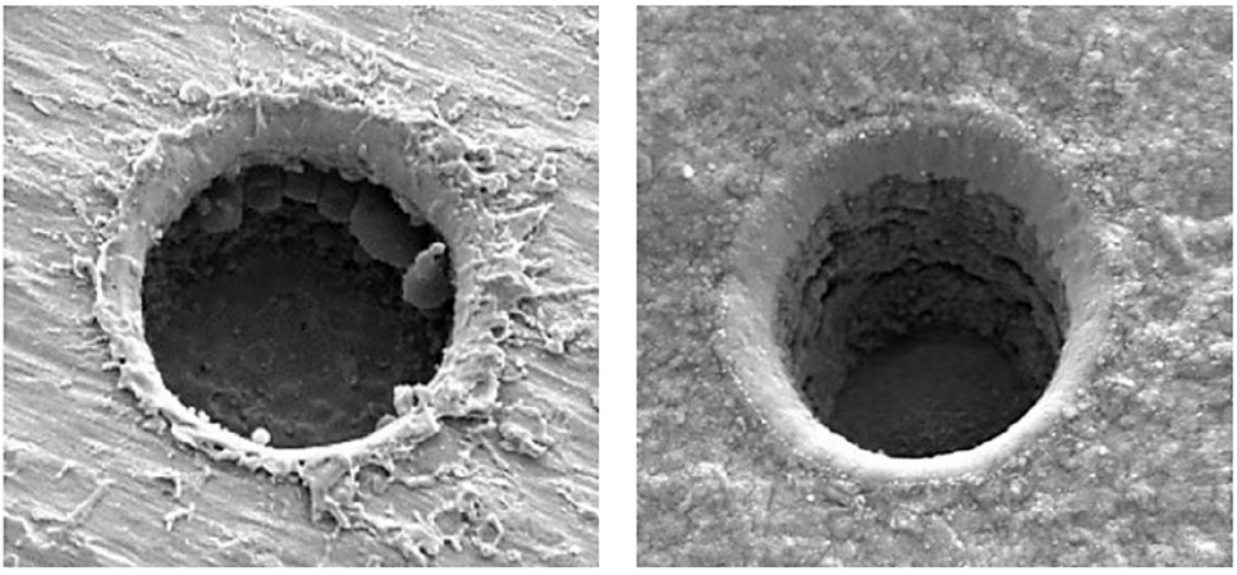


Figure 4: Typical microvias formed with nanosecond laser (left) and USP laser (right). (Source: Orbotech)

second pulses with picosecond or femtosecond pulses. These offer not only smaller vias but do so with a much smaller HAZ, meaning microvia pitch can be greatly reduced and as laser absorption is improved, the resulting vias are of a much better quality with less surface debris or "splash." As these laser systems become available, the capability of microvia density will take a step improvement, enabling another jump in HDI capability.

Once the microvias are formed, the next issue becomes plating, and while vias have not had dramatic changes in aspect ratio, typically maintaining 0.7-0.8, they have steadily reduced in size, which has led to challenges in plating. One important development has been the ability to fully fill vias with copper, which has enabled the stacking of vias directly on top of each other. This has been so influential that stacked vias are an integral part of HDI design as they enable space savings, especially over the older staggered vias, improved thermal and electrical management, and their superior surface planarity also contributes to final assembly yields.

One recent plating development has been the release of processes for through-hole filling (THF). Solid columns of copper will improve thermal conductivity in heat-critical areas allowing for improved cooling and THF potentially supports increased I/O density as via-in-pad is still possible.

BGA Design Rules

As in many cases, the critical design parameters for an item are often linked to other aspects within that design, and HDI PCBs are no different. In this case, some of the controlling factors are the BGA pad size and pitch.

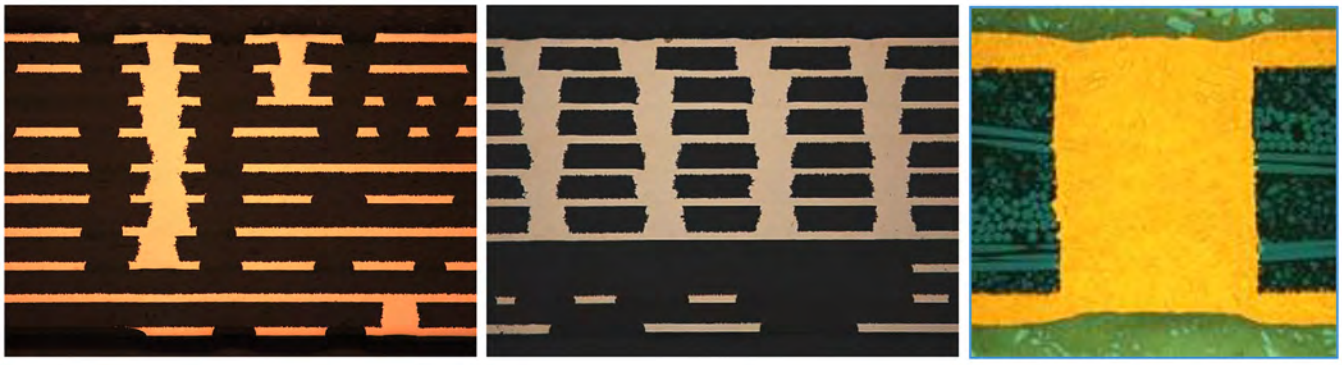


Figure 5: Stacked microvia and through-hole filling.

Number of Traces	Required Line / Space Width
1	g ≥ Line Width + (2 x Space Width)
2	g ≥ (2 x Line Width) + (3 x Space Width)
3	g ≥ (3 x Line Width) + (5 x Space Width)

Table 1: L/S required for given pad dimensions.

Looking at Table 1, we can see the relationship between solder pad dimensions and possible trace widths, depending on the number of traces required to pass between the pads. For a "simple" or low I/O count package (Figure 6a) where we only need to route a single trace in-between the BGA solder pads, it's clear that the maximum trace width is 1/3 of the available space between the pads. In the example shown, we have 300 µm pad pitch, with 150 µm pad diameter, resulting with a recommended line and space requirement of 50 µm.

If we now use a more complex package where the higher I/O count requires that two traces need to route through the same pad spacing, the recommended L/S drops to 30 µm, and it's obvious that as pad pitch decreases, this will apply further restrictions for line width and separation.

As a general summary, the availability of new laser tools will allow for smaller microvias that will be closer together. This will help enable the use of smaller solder pads on the BGA,

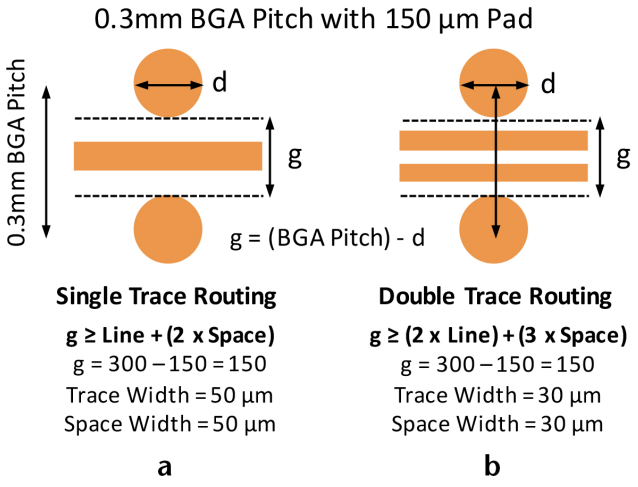


Figure 6: Effect of trace count on dimensions. (Source: Altera)

and in combination with higher I/O count devices, will drive the demand for a reduction in line and space requirements, which will push the HDI roadmap (Figure 7) and continue the move from the existing every-layer production routes into the variations of the semi-additive processes.

ELIC, Any-Layer and mSAP

The majority of HDI PCBs are currently produced using a subtractive ELIC (every layer interconnect) or any-layer technique. The general process flow is outlined in Figure 8.

There is a demand for high-end HDI PCBs to move from 40 µm L/S down into the region of 30 µm, and as this can not be achieved with

	2015	2016	2017	2018	2019	2020
µVia Diameter (µm)	70		50		40	
µVia Aspect Ratio	0.8			0.9	1.0	
µVia Pad Diameter (µm)	200	140	140	130	120	100
Min L/S (µm)	35/35	25/25			20/20	
Cu Thickness (µm)	15	12	10			8
BGA Pitch (µm)	350	300		250	200	
Technology	Subtractive		mSAP/aMSAP			

Figure 7: Critical factors within the HDI Roadmap. (Sources: IPC, Jisso, Atotech, customer base)

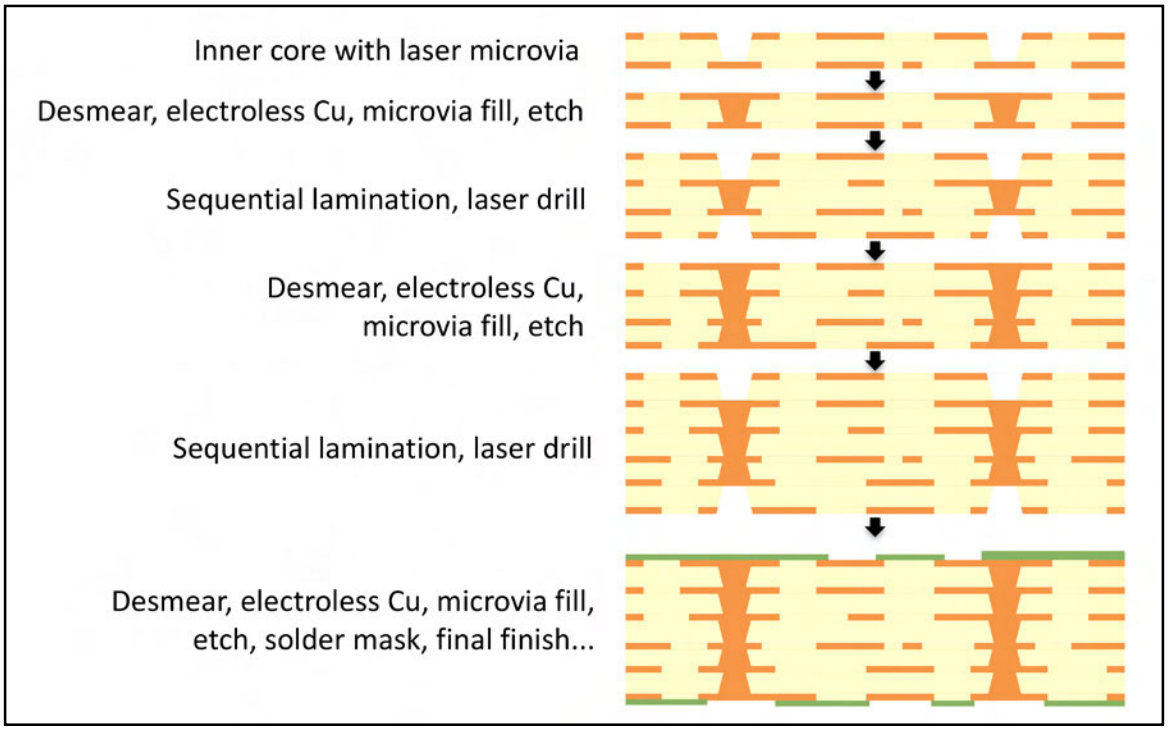


Figure 8: General schematic for the ELIC process flow.

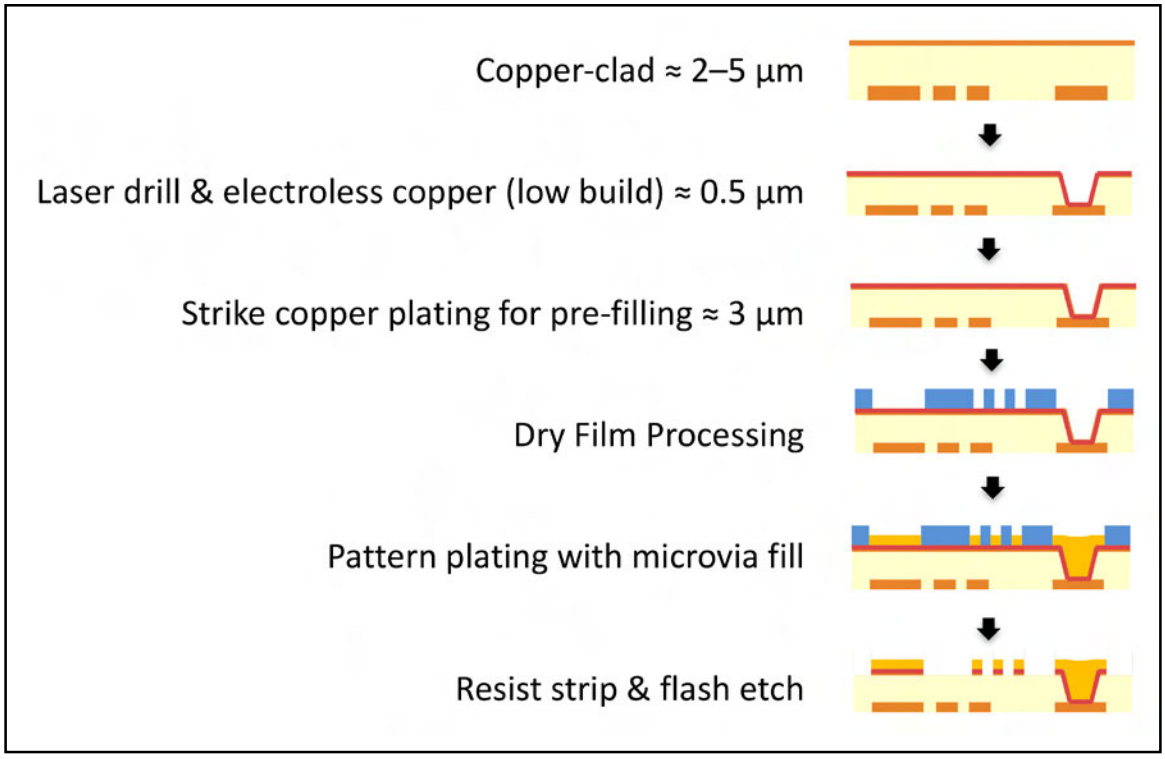


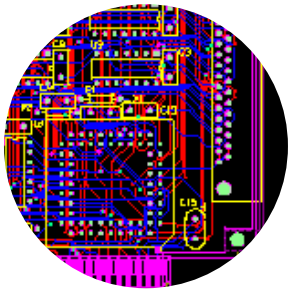
Figure 9: Outline schematic for SLP process based on mSAP.

the current panel plating process, a switch to semi-additive processes is required. With these processes being common to IC substrate production, the resulting HDI boards are becoming known as substrate-like PCBs (SLP).

A generic process flow for SLP production based on mSAP techniques is shown in Figure 9.

Having trouble keeping up with front-end demand?
We have people for that.

Here are six ways that outsourcing CAM and related front-end work can help manufacturers not only stay in business but also help them thrive:



- **Increased on-demand capacity**
- **Improved automation**
- **Faster turn-around times**
- **Reduce costs**
- **Improved quality**
- **Ability to build redundancy in critical areas**

We deliver the highest quality PCB CAM and Mechanical CAD engineering services to customers around the world.

Find out how we can help you >

ENTELECHY GLOBAL

www.entelechyglobal.com

Process Challenges

It is clear that the mSAP processes share common steps with the more traditional PCB production routes, so in principle it would appear to be quite straightforward to update and stretch existing facilities in order to make the change from subtractive to mSAP production. However, due to many of the changes involved, it is typically seen as simpler, and as has been proven recently by those vying to enter the SLP supply chain, certainly better to make the required investment into new equipment and processes which are tailored to the mSAP approach. One obvious concern after such an investment would be the expected lifetime of the mSAP processes. Fortunately, these can be further revised into an amSAP approach, which enables >20 µm L/S with limited further investment being required.

Table 2 shows a simple comparison of the technologies available, including their capabilities and major differences.

For those looking to enter the SLP supply chain and begin to provide suitable boards, there are a number of challenges that need to be overcome, some of which can be resolved through investments, others which can only be achieved through working with experienced process suppliers.

Improved Laser Drilling

While the new generation of laser drill tools will surely arrive in due course, the current CO2 machines will remain the workhorse of microvia processing for some time. Updated for compatibility with the reduced foil thickness used in mSAP, chemical processes can pretreat Copper surfaces to maximize CO2 laser absorption and achieve improved hole shape, while ensuring the best possible conditions for subsequent plating operations

Optimized PTH

Reliable PTH coverage in microvias is critical to not only mSAP production but the anticipated reduction in via dimensions, along with a broadening range of dielectric materials, means that the electroless copper processes will also require review. Robust activation systems combined with optimized pretreatment systems will be required to work with high throwing power electroless copper baths to ensure via coverage, be that in vertical or, as is more common, horizontal tool sets.

Pattern-Plated Copper

Filled vias, be they full through-hole or stacked microvias, are essential to modern mobile PCB designs. However, for SLPs via fill must be achieved along with fine line pattern plating and excellent surface uniformity, all within acceptable plating times.

Fine Line Formation

<30 µm lines require fine line imaging processes not typical to subtractive processing.

	Subtractive	mSAP	amSAP	SAP
Achievable L/S (µm)	> 35	> 30	> 20	9/12
Cu clad thickness (µm)	2–9	2–5	< 3	
E'less Cu thickness (µm)	0.35–0.50	0.35–0.50	1	1
Flash Cu thickness (µm)	2–5	1–3		
Panel plating thickness (µm)	15–20			
Pattern plating required	No	Yes	Yes	Yes
Etch resist	Dry film or LER			
Cu to be etched	17–29	4–10	< 3	0.7–1.2 (Rz)

Table 2: Outline comparison of PCB production techniques.

ISO 9001 Quality Management

AS-9100D

PROTOTRON.COM
(888)847-7686

Your Passport to Global PCB Sourcing

We are pleased to announce that with the same fine service, quality, delivery and attention to detail that our customers have grown to rely upon, we are now adding a complete global solution to meet all of your needs, both today and in the future.

Our Solutions:

- *FLEX & RIGID-FLEX*
- *HDI / MICROVIA*
- *COMPETITIVE VOLUME PRICING*
- *PRE-QUALIFIED OFFSHORE PARTNERS*
- *QUICK-TURN PROTOTYPES*
- *COMPLEX MULTILAYER*
- *MIL-SPEC PRODUCTION*
- *SPECIALTY MATERIALS*

LEARN MORE
PDF DOWNLOAD

Prototron Circuits

A COMPLETE GLOBAL SOLUTION

REDMOND, WASHINGTON • TUCSON, ARIZONA • GLOBAL PARTNERSHIPS

Low etch surface preparation aids with dry film adhesion, novel resist strippers are needed to ensure no film residues, while controlled etch processes must be able to form the final patterns without excessive undercut or track width loss

Improved Layer Bonding

With finer patterns, higher track densities and the push for higher operating frequencies, SLP processes must minimize copper removal and maximize signal integrity through low surface roughness where possible.

High-Resolution Surface Finish

With finer features across the SLP, the final finish must also ensure compatibility, and in most cases this means no extraneous plating (nickel foot). This, in combination with enhanced corrosion resistance and controlled gold thickness, makes the new generation of ENIG chemistries the preferred solution for high-end PCB applications.

Summary

With more mobile device designers looking to utilize the benefits of FOWLP and other direct attach package types, a new generation of HDI PCBs is already in the market. Targeting < 30 µm features and based on mSAP techniques, these substrate-like PCBs make use of the latest high-end manufacturing processes and materials, to enable the next evolution in advanced HDI boards.

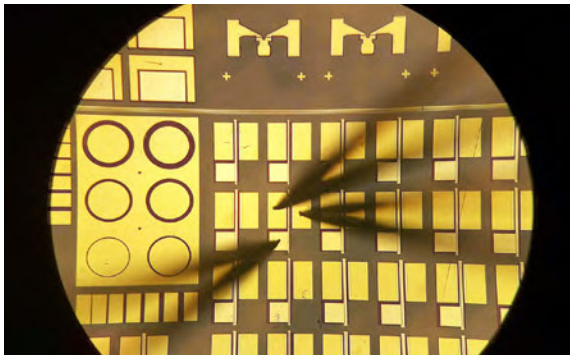
Chemical and material suppliers are realigning processes and products from the packaging industry and adjusting them to fit into this new SLP sector, while prospective SLPs producers are reviewing their existing processes and deciding if they should invest. As some will inevitably decide against the investment, will we risk a limit in the future numbers of players in the SLP supply chain? Only time will tell, but the advanced HDI market is again facing a new challenge, but one we can surely rise to meet. **PCB007**

Roger Massey is technical marketing manager at Atotech GmbH.

The Electronic Transistor You've Been Waiting For

How do you pack more power into an electric car? The answer may be electronic transistors made of gallium oxide, which could enable automakers to boost energy output while keeping vehicles lightweight and streamlined in design.

A recent advancement—reported in the September issue of the journal *IEEE Electron Device Letters*—illustrates how this evolving technology could play a key role improving electric vehicles, solar power and other forms of renewable energy.



"To advance these technologies, we need new electrical components with greater and more efficient power-handling capabilities," says the study's lead author Uttam Singisetti, PhD, associate professor of electrical engineering in UB's School of Engineering and Applied Sciences. "Gallium oxide opens new possibilities that we cannot achieve with existing semiconductors."

The most widely used semiconducting material is silicon. For years, scientists have relied upon it to manipulate greater amounts of power in electronic devices. But scientists are running out of ways to maximize silicon as semiconductor, which is why they're exploring other materials such as silicon carbide, gallium nitride and gallium oxide.

While gallium oxide has poor thermal conductivity, its bandgap (about 4.8 electron volts) exceeds that of silicon carbide, gallium nitride, and silicon.

Bandgap measures how much energy is required to jolt an electron into a conducting state. Systems made with high-bandgap material can be thinner, lighter and handle more power than systems consisting of materials with lower bandgaps.

(Source: University at Buffalo)

JOIN IPC'S JOB TASK ANALYSIS COMMITTEE

Make sure your voice is heard on the critical issue of skills gap in the electronics manufacturing industry. Help IPC define the workforce skill requirements needed for today and the future.

Join **IPC's Job Task Analysis Committee (JTA)** to help address the skills gap and provide training and career opportunities for your employees.

Why Join JTA?

- To address the skills gaps in your own company.
- To ensure that your staff will be well trained moving forward.
- To decide which jobs need focus and which skills are most important for your industry.

Help us help you shape IPC education and certification offerings that keep your company moving forward and improve recruiting and retention.

For further information, please contact **Dave Hernandez**, senior director of learning and professional development, at **davidhernandez@ipc.org**.

Supplier Highlights

Gardien Launches Largest Operational Tester in the World ▶

Gardien Group debuts G90 XXL—the biggest operational tester yet in North America. With a maximum board size of 63" x 47.2" (1600 mm x 1200 mm), this premium double-sided flying probe system is set to create a revolution in the industry.

Ventec International Group Appoints Jason Chung as CEO ▶

Ventec International Group Co., Ltd. announced that its board has elected Jason Chung as group CEO with immediate effect. Chung succeeds Tony Lau who continues in his role as chairman of board of directors.

American Standard Installs Hitachi Drill ▶

American Standard Circuits has recently acquired and installed a Hitachi Drill Model ND-6Y210E. The Hitachi ND-Y series demonstrates high-speed and high-precision drilling powered by an advanced servo system.

Punching Out! Beware of Customer Concentration Risk ▶

One of the biggest risks in M&A is customer concentration risk. It is hard to avoid as a business owner; if a customer is giving you orders, you generally take them! The next thing you know, your customer has 90% of your sales and they own you. We see this a lot in both the PCB and contract manufacturing industries.

Circuit Automation on the Ever-Evolving World of Solder Mask ▶

In a recent conference call, I-Connect007 editorial team was joined by Circuit Automation's Yuki Kojima, VP of engineering; Larry Lindland, sales and applications manager; and Tom Meeker, CEO, for a lively discussion about solder mask. Spoiler: It's not all about the equipment.

First EIE Technology at Royal Circuits ▶

Royal Circuits Group has furthered its investment in First EIE process equipment, acquiring a direct image system for its facility in Southern California, and inkjet technology for the Hollister, Northern California location.

Agfa: Staying Ahead of the Technology Curve ▶

In the ultracompetitive electronics manufacturing space, companies that don't continually evolve and invest in new technologies run the risk of being left behind. At the recent EIPC summer conference, many next-generation processes and technologies were discussed and even put on display.

A-Gas Electronic Materials Acquires Elga Europe ▶

A-Gas Electronic Materials have acquired all the assets of Elga Europe of Daventry in Northamptonshire. Elga Europe is the sole dry film distributor of Ordyl film in the UK, which is used extensively in printed circuit board manufacturing and currently produced and slit in Milan at Elga Srl.

R&D Altanova Chooses Ultra-Precision atg S3-8 - Flying Probe Technology for High-Speed Electrical Test of Substrate Products ▶

atg Luther & Maelzer GmbH, confirms delivery of high-speed bare board testing technology to R&D Altanova.

Integrate QA Solution

Because everyone's QA needs are just a little bit different.

Integrate is a fully customized solution, and no two contracts are exactly the same. No matter what size customer you are, we can tailor AOI, testing, final inspection, or a combination of all three services to fit you. And you only pay for the product that actually passes quality assurance, not on panels produced or tested.

Find out if our Integrate solution is right for you!
www.gardien.com/why-integrate

GLOBAL FOOTPRINT
WITH A LOCAL PRESENCE

30+ YEARS
EXPERIENCE

30 YEARS OF PCB
INDUSTRY EXPERIENCE

Catching up with... James Rathburn

President, HSIO Technologies

Feature by Dan Beaulieu

I love innovative companies and keeping up with what they are doing. One of the most creative and innovative companies in our industry is HSIO Technologies, founded by entrepreneur and inventor James Rathburn. Based in Maple Grove, Minnesota, this company stays at the cutting edge of the electronics industry's technology. Leveraging extensive interconnect device knowledge with proven semiconductor fabrication, printed circuit fabrication, and microelectronic assembly processes enables them to quickly develop cost-effective, high-performance interconnect solutions across a wide variety of form factors. I checked in with Jim recently to see what he and his team are up to and learned how they are using liquid crystal polymers and other materials to focus on increasing high-speed and high-density PCBs for uses in all markets.

Dan Beaulieu: Jim, for the readers who might not be familiar with HSIO, tell us a little bit about it.

James Rathburn: I founded the company in 2010 and launched it with an investment from partners from a previous company called Gryphics Inc., which we sold in 2007. The previous company produced high-performance test sockets for the semiconductor industry. The customer base was reaching a point where the signal integrity of the system PCB and package substrate were defeating the performance of the high-speed sockets. The plan was to create an integrated technology that would include high-speed printed circuits with low-loss connectors, to mate them. We started HSIO by going to our customer base and asking, "If you could have new technology developed, what would that be?" The common theme was that they needed finer lines and spaces. They also said that vias were killing their signals. So, from that came our charter at HSIO which was to come up with a new way to look at fabricating printed circuits with finer lines and spaces and signal integrity as the focus.

Beaulieu: What are some of the ways you are meeting those challenges, with respect to technology at HSIO?

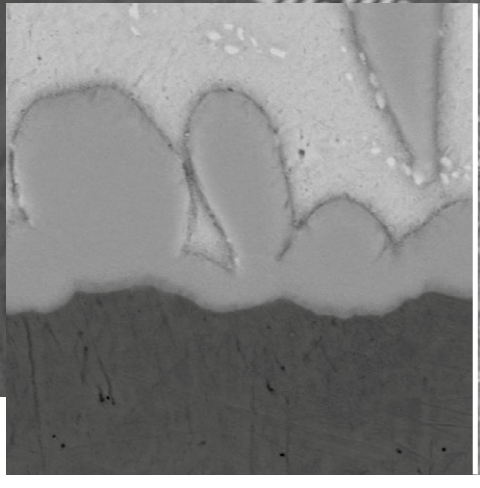
Rathburn: We are in the process of commercializing a printed circuit technology we have developed utilizing liquid crystal polymer technology. The technology is not limited to LCP, and we can utilize conventional materials, but LCP is the focus for high-speed and high-density. We developed the technology in our Minnesota and Arizona operations and have established a manufacturing relationship with Benchmark Electronics to scale production and

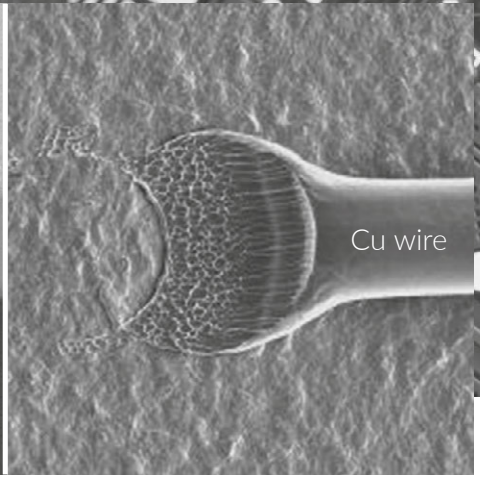
PallaBond®

Premium soldering and wire bonding capability

ATOTECH

Direct pure EPAG for real fine L/S application





IMC investigation
0.1 µm Pd / 0.1 µm Au

Top view: copper-wire
20 µm on EPAG finish

PallaBond® is an environmentally friendly process suitable for high frequency and fine L/S applications. The process provides very good bonding capability with aluminum-, gold-, silver-, copper- and copper-palladium-wires. Especially outstanding is its good solder joint reliability.

Thanks to its very mild process conditions, it provides excellent compatibility with base materials and soldermasks. It also consumes less energy and water than ENIG, ENEPIG and immersion tin finishes.

Bio compatible pure palladium ideal for medical application

Atotech Group
+49 30 349850
info@atotech.com

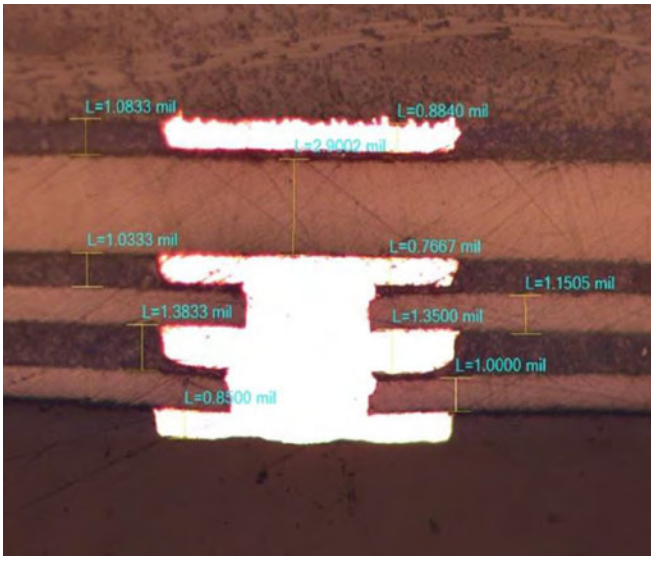


Figure 1: 12-layer LCP PCB with hybrid rigid core and LCP high-speed signal layers.

support engineering and application development. Benchmark is launching full production with the RF High-Speed Design Center of Innovation, circuit fab, micro-electronics assembly, SMT assembly and test—all within the same process flow, all focused on next generation high-speed and RF technology needs. We are very proud to be part of this effort, which has never been done this way in the EMS industry. We work directly with the Lark RF Technology subsidiary of Benchmark, and Daniel Everitt, Benchmark's VP and GM of Lark, will be presenting at the upcoming EDICon conference in October.

Beaulieu: Why did you choose to go in this direction?

Rathburn: The original development plan was to create a circuit-plus-socket technology family with tuned performance for the semiconductor test customer. Historically, the chip producer tests the device to make sure it will function properly in the final system. Typically, the signal integrity requirements for test have been much more stringent than actual system use to make sure everything in the system works together. As system performance and complexity has evolved, in many cases it is no longer good enough to test outside of the actual usage model. This development has evolved further to the point where many end systems need to have the performance previously needed only at test. Our technology can provide the best performance in both test and commercial markets. In the end, the purpose of the technology is to provide a new way of designing and fabricating high-performance printed circuits with high-density.

Beaulieu: What markets are interested in using this technology?

Rathburn: One of the most exciting aspects of the technology is the various markets it can apply to. In the past, the mil/aero/defense/satellite/space/test industries were the main drivers of RF and MW technologies. In the world we have today and in the pending future, high-speed digital, mobile/wireless, automotive, low-power mixed signal, and analog technologies all kind of need the same precision circuitry fabrication techniques. From aerospace and defense, to consumer electronics, to medical markets, the principles of size reduction with performance improvement available from a company like Benchmark that can design, produce and test volume is very compelling. The best part from a design perspective is the technology is basically the same regardless of the market.

Additionally, there is a broad range and mix of industries we are working with. The milaero/defense industry is probably the area that has lacked this type of capability to date and there is a large focus in the community towards heterogeneous integration and advanced packaging. These types of engagements typically start with an incumbent technology with evaluations as to how to make the existing better near term then explore longer term qualification with a more integrated approach. High-speed data, processing, memory, wireless/RF applications all have interests that are much shorter life cycles and driven by systems and silicon development.

With the onset of 5G deployments, smart vehicle and automotive communications, flexible displays, high-speed data/optical processing and storage along with the mil/aero needs,

I call the future a technology convergence. All those industries need the same technology, just in a different configuration, scale and volume. Everyone needs to worry about high-speed signals, power requirements, thermal management, physical size, cost, antennae, filters and mixed-technology hybrid assembly. LCP is also rather unique in that it has low moisture absorption and has the potential for exposed environments, hermetic applications and implantable medical devices.

Most of our efforts currently are aimed at characterization with design rule and manufacturing refinement out to 110 GHz RF and 112 GB digital. As with any new technology, there is a period of time required for dialing in the design rules and refining the production processes needed to ramp volume capability. Long-term reliability requirements vary greatly from market to market and that is of key interest to all. Component obsolescence in the mil/aero industry has also become a major issue. By the time a program launches, oftentimes one or more silicon nodes have passed the technology by and there is significant interest in the ability to take state of the today's technology components and arrange them in a meaningful way that fits into a legacy platform without full requalification.

Beaulieu: Jim, let's dig a little deeper. What can you tell me about the some of the specific capabilities of your products?

Rathburn: When you look at the current line and space capability in the domestic supply base, there are many companies that can produce high-quality 3- to 4-mil line and space multilayer circuits. There is a challenge to produce high-speed multilayer boards with very tightly controlled impedance below 2-mil line and space with conventional materials, and there has been a domestic supply chain gap. LCP has been around for many years but has suffered from reliability and density challenges with multilayer applications. The production launch capability can fabricate 1-mil or 25-micron line and space LCP circuit stacks with up to as many 20 layers in flex, rigid-flex, substrates, modules and multilayer boards. We are also launching our next generation technology that pushes the line and space capabilities to nine microns, with added capabilities like embedding coaxial signal lines, embedding active and passive components and high-speed functional test at the die level during assembly.

Beaulieu: Tell our readers something about your and the team's expertise.

Rathburn: Our expertise at HSIO is fundamentally electrical interconnects but extends to understanding how our customers need to interconnect everything in a system, not only today but in the future. The next step is to create a technology that is based on sound manufacturing processes but also not just another version of what is already available. The material LCP has some great properties, but it is the way it is used as part of the manufacturing process that

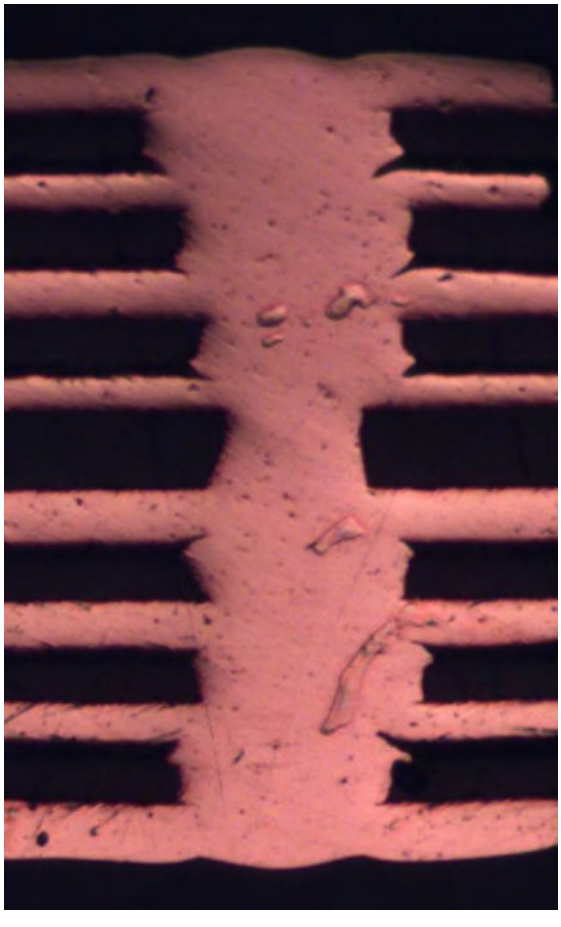


Figure 2: Cross-section of 12-layer LCP rigid-flex with solid full metal microvias.

is the key. The ability to take advantage of the process capabilities with design and application expertise to help customers convert traditional designs or create brand new ones is critical to market acceptance as well. This is what the Benchmark relationship is all about.

Beaulieu: One of the things I always look for in a company is what makes them outstanding. What is it about HSIO that makes them outstanding?

Rathburn: Our technology has been very well-received by an impressive list of customers across many market segments. The engineering communities can solve challenges and create new ways of integrating electronics components into a package, or higher-level assembly. Traditional high-performance materials are typically expensive and actually reduce the density of interconnect in many cases when pushing to higher frequencies. Our approach allows for higher-tuned performance while increasing the density and reducing the effective product size. The ability to embed components that are normally surface mounted is a large focus for the future. Benchmark is enabling the entire capability chain to help customers with engineering expertise focused to take best advantage of the technology from concept, through production, as far as the customer would like to go, all the way to system and box build. Many customers can envision multiple generations of integration with enhancements rather than brand new design, which is very significant from a time-to-market and development standpoint. We believe that once the technology is adopted, there is no going back to previous generations with conventional materials and methods. I think what makes HSIO stand out is we have very good relationships with the test and development groups within the leading semiconductor companies. Our products are used to test many of the future chips 1–3 years before the devices that use those chips enter the market. We see the system requirements driven by the next-generation chip technology needs long before any printed circuit supplier or EMS company would. Providing the technology and high performance needed for silicon validation and system level test and enabling those capabilities in volume production end-product use is a major goal of the Benchmark-HSIO relationship.

Figure 3: Cross-section of coaxial signal lines embedded in LCP circuit stack.

Beaulieu: Where do you rate HSIO's products and technology compared to the competition?

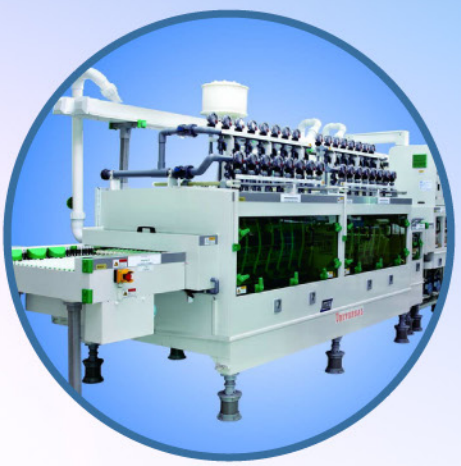
Rathburn: Our main competition is the conventional material sets and design rules. Most engineering teams would rather extend what is already being produced to meet the next generation requirements. Another competitive aspect is that LCP as a material has been an elusive treasure that has a bad reputation for being difficult to process, hard to control, and unreliable in the field. Volume use within the cellphone market in recent years has helped overcome reluctance and our technology demonstrations are possibly the most impressive LCP products built.

The technology convergence I mentioned is creating multiple roadblocks across multiple industries; that is a huge challenge, but also a significant opportunity. As signal speeds and frequencies jump from today to multiples of today in the next couple of years, it is not only important to function at the desired base frequency, but the accuracy of the circuits in the band around that frequency is equally, if not more, important. Our philosophy is "every micron matters" and that is truly the case

UCE WET PROCESS LINE

Etchers

Scrubbers



Developers

PTH

Oxide Replacement

THIN CORE HANDLING • PC CONTROL • RELIABLE • LOW COST

CLICK TO VIEW OUR UCE WET PROCESS LINE

The leading European PCB Equipment and Parts Supplier

www.vikingtest.com
sales@vikingtest.com

Viking

when tuning very fine, high-density circuits in a stack that may have 12 to 20 layers. Traditional PCB suppliers in the U.S. often still communicate in mils and have a somewhat experience-based view of build-to-print and acceptable geometries. At the same time, if the application can get by with 3-mil lines and spaces on polyimide or FR-4, then we are not the right fit. Many of the industry publications and conferences highlight state-of-the-art modified semi-additive substrates or wafer level fan-out packaging for high-volume applications. We believe our technology has the right mix of fine lines, impedance control, layer count and the expertise Benchmark provides for engineering, production, assembly and integration that is found nowhere else.

Beaulieu: Now let's talk about quality. Let me know what qualifications, certifications and registrations you have and why these give you an advantage over other companies.

Rathburn: One of the challenges HSIO faced as a company developing promising technology is that the engineering teams have interest and the ability to experiment and explore, but commodity and production teams need a viable, strong supplier base to even consider important components. Historically, customers in the test and development world are less concerned with volume production, certifications, ISO registrations and that is the market HSIO has served directly in the past. A key advantage of the Benchmark relationship is they are a respected tier EMS company that has the strength, reputation, qualifications and resources to support customers across most markets with all of the commercial requirements along with the leading-edge technology and capability that sets them apart from commodity PCB assembly and box build.

Beaulieu: Jim, I know that much of your work is considered research and development; can you talk about that?

Rathburn: Our R&D work is typically driven by a specific customer need that can be applied to multiple customers and multiple markets. We try to avoid science projects that are for the sake of R&D and focus on process development that can help us make something meaningful. We are launching the LCP technology product at the 25-micron range node and that is a significant improvement with multiple shrinking of conventional technology and significant opportunity.

The focus of our current R&D efforts is what I call Direct Die Attach LCP. The principle is to arrange packaged components without the substrate or interposer and attache the die directly to an LCP module. The evolution is to shrink the current PCB assembly with an LCP PCB, then shrink one step further with direct die attach. The DARPA CHIPS program has a similar philosophy to disintegrate an ASIC device into chiplets that can be assembled onto a substrate and offers the capability to include mixed semiconductor technology beyond monolithic silicon. Our parallel R&D effort is the ability to test these devices at speed as a connected group before they are assembled, while they are being assembled, and after they are assembled. Known good devices are important in this type of assembly, and critical if devices are embedded within an assembly with no possibility of rework.

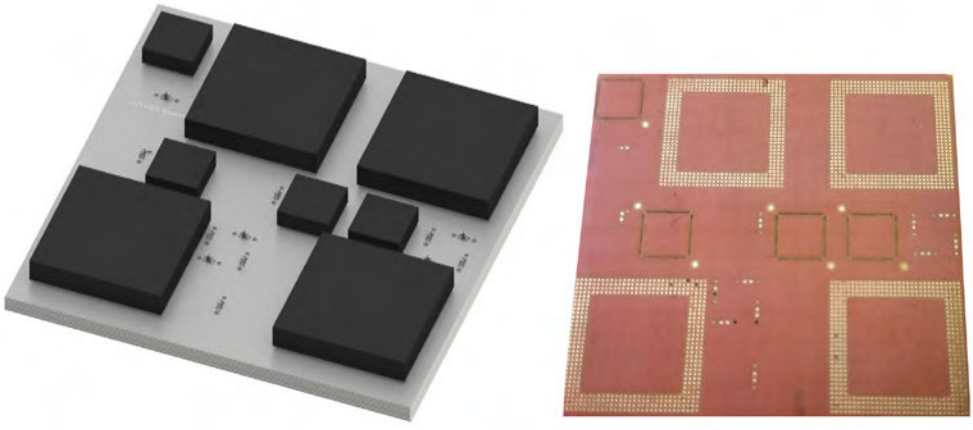


Figure 4: 10-layer LCP substrate PCB with hybrid SMT assembly and flip chip die attach.

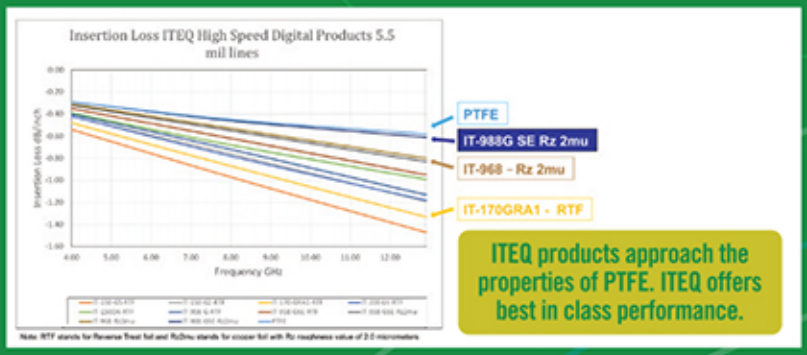
IT-968 / IT-968 SE

High Thermal Reliability
Designed for High Speed Digital Applications
- Telecom, Backplane, Base Station, Server, Storage, Switch

IT-968
Dk @ 10 GHz - 3.85
Df @ 10 GHz - 0.0043

IT-968 SE
Dk @ 10 GHz - 3.30
Df @ 10 GHz - 0.0019

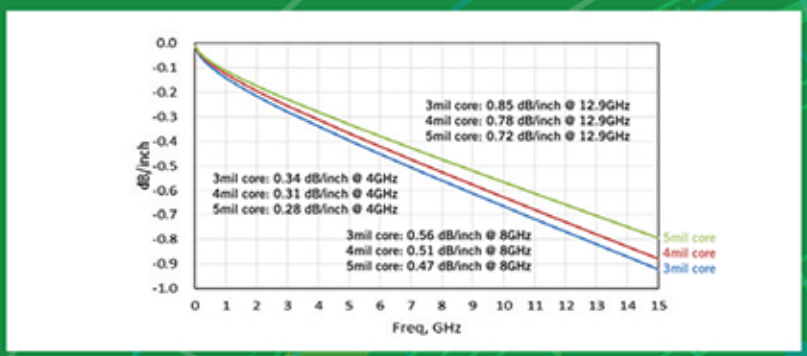
Insertion Loss - Measured



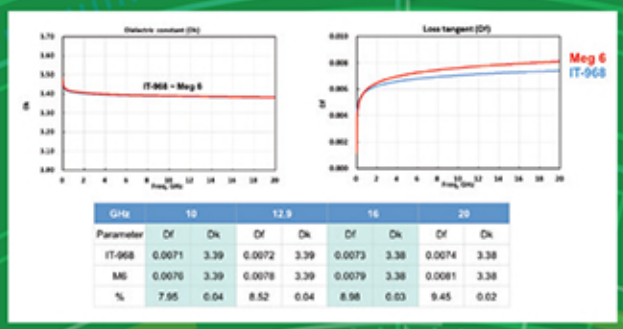
Industry Test Vehicle

32 layers, 0.140" thick
Four 2 oz copper internal layers
0.8 mm pitch, 9.8 mil drills
- Passed 1000 hours CAF, 10 V bias, 50 V
- IST - Passed 1000 cycles, 6x 260°C precondition
- No delamination after 8x 260°C reflow after 2 weeks at 35°C/ 85 % RH

IT-968 Loss Performance

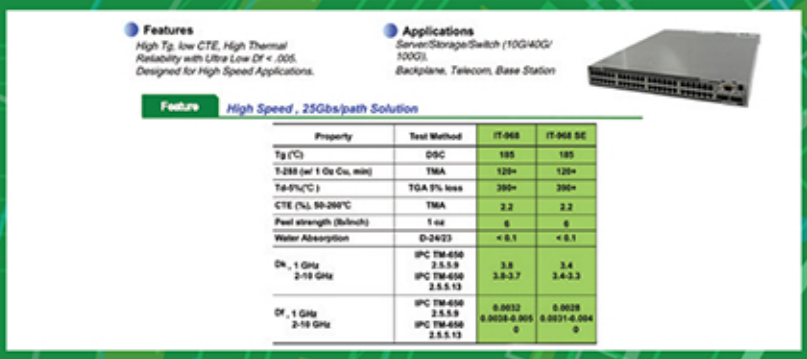


IT-968 SPP Comparison



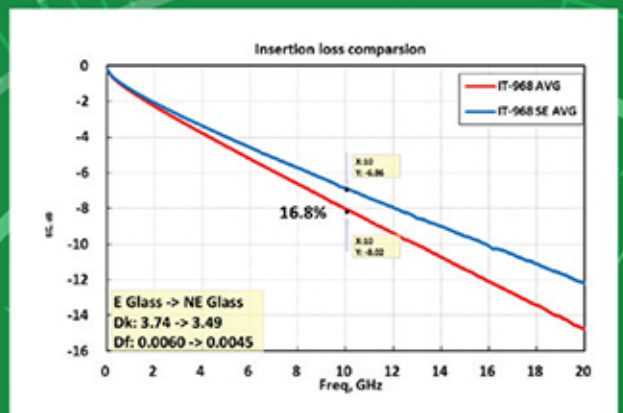
GHz	10		12.9		16		20	
Parameter	Df	Dk	Df	Dk	Df	Dk	Df	Dk
IT-968	0.0071	3.39	0.0072	3.39	0.0073	3.38	0.0074	3.38
M6	0.0070	3.39	0.0078	3.39	0.0079	3.38	0.0081	3.38
%	7.95	0.04	8.52	0.04	8.98	0.03	9.45	0.02

Ultra Low Loss IT-968 SE



Property	Test Method	IT-968	IT-968 SE
Tg (°C)	DSC	185	185
T-288 (w/ 1 Oz Cu, min)	TMA	120+	120+
Td-5%(°C)	TGA 5% loss	390+	390+
CTE (%), 50-260°C	TMA	2.2	2.2
Peel strength (lb/inch)	1 oz	6	6
Water Absorption	D-24/23	< 0.1	< 0.1
Dk , 1 GHz 2-10 GHz	IPC TM-650 2.5.5.9 IPC TM-650 2.5.5.13	3.8 3.8-3.7	3.4 3.4-3.3
Df , 1 GHz 2-10 GHz	IPC TM-650 2.5.5.9 IPC TM-650 2.5.5.13	0.0032 0.0038-0.005 0	0.0028 0.0031-0.004 0

E-Glass vs Low Dk Glass



ITEQ

Figure 5: Benchmark's RF High-Speed Design Center, circuit fab, and assembly operations.

Beaulieu: What are your plans? Where, for example do you want to be in five years?

Rathburn: The short answer is five years away seems too far away to predict. The drive for silicon node shrinks appears to be more challenging and yield curves difficult to manage. When I look at today's state-of-the-art electronics, there are extremely complex silicon devices surrounded by hundreds of less complex devices and connected with large connectors. We have many patents, applications and disclosures related to high-speed interconnects that can not only improve the performance and shrink the PCB, but also the internal connectors and interfaces to the outside world. The elegant integration of these complex interconnects in a high-speed way is my personal interest. The plan driven by reality today is to support the production ramp, work with customers to design their version of the technology and push the capability to the next node in 2019.

Beaulieu: What new products are your working on?

Rathburn: We are currently investing in two parallel paths. The first is engineering and applications support for Benchmark customers as the technology matures and is adopted into production. Benchmark has made significant investments in the launch technologies that will be available in production soon, but the engineering expertise to help the customers implement is a key future investment with software, simulation, high-speed and RF design rules, and practical application support.

The second investment is to extend the launch capability to the next process node with a key focus on not just the circuit fabrication, but the unique assembly techniques needed to integrate function and devices into the LCP circuit stack. Shrinking from 20- or 25-micron circuit fabrication down to nine microns does not seem like a big shrink, but below 20 microns there is a significant process and capability shift that is not trivial.

Beaulieu: When will they be coming out?

Rathburn: The launch capabilities are in sample and qualification stages through 2018, and 2019 will bring the next technology node.

Beaulieu: Any last comments as we wrap up this interview?

Rathburn: In closing, HSIO is very proud to be in a position to enable our exciting technologies with Benchmark as our manufacturing partner, and our customers as our development partners. There is no other company, collaboration or technology I am aware of that can design, build and assemble a high layer count, high-density, high-speed LCP-based printed circuit with the ability to directly attach die or embed devices that normally function discretely. We are also very proud to be a foundational part of Benchmark's new RF High-Speed Center of Innovation and believe our vision and technologies are fulfilled in a way that makes Benchmark the new measure in the EMS industry.

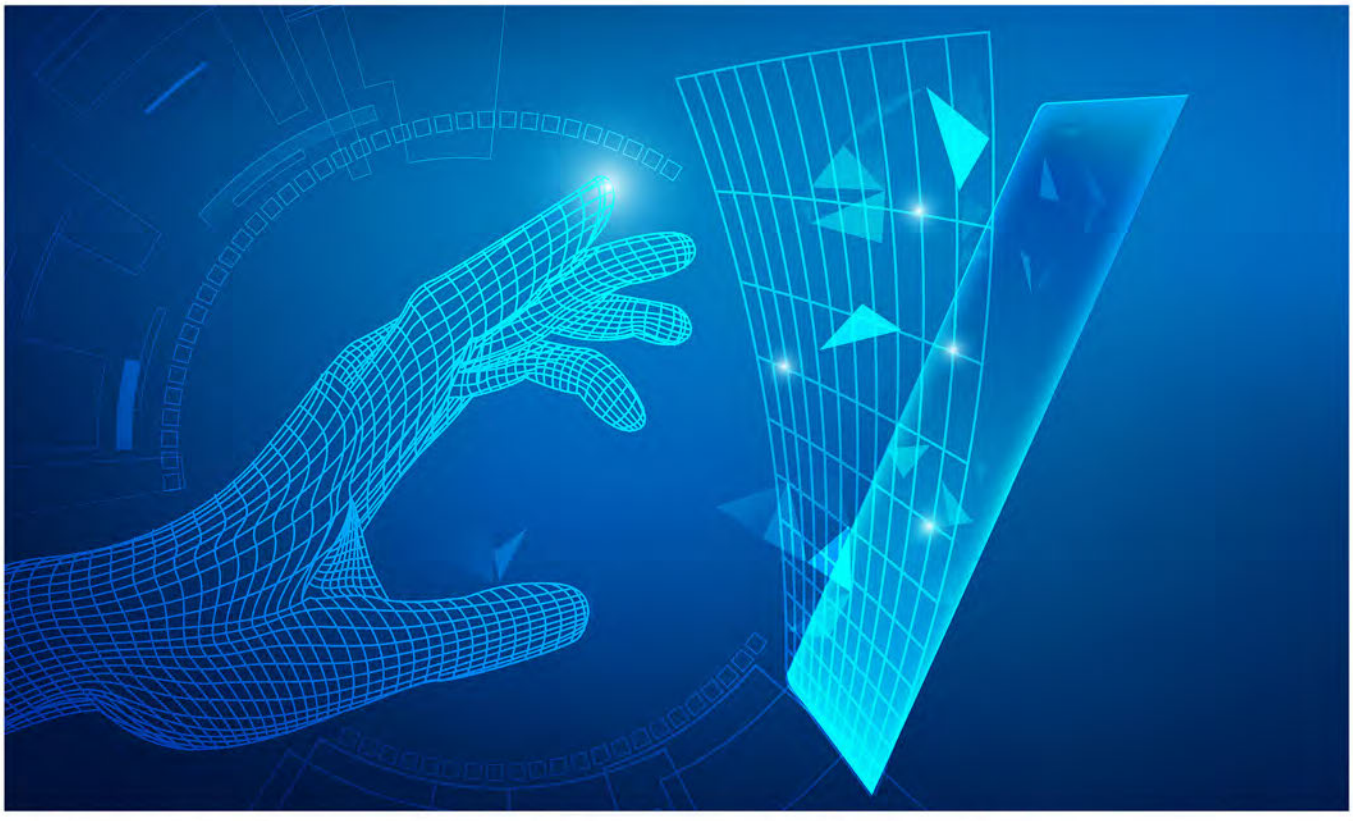
Beaulieu: Thanks, Jim. **PCB007**

A NEW QUARTERLY MAGAZINE

With original content dedicated specifically to flex system and PCB designers, electrical engineers and those responsible for integrating flex into their products at the OEM/CEM level, you won't want to miss a single issue of ***Flex007 Magazine****!*

Subscribe **Contribute** **Advertise**

I-Connect007
GOOD FOR THE INDUSTRY



Smartphone Substrate-Like PCBs Will Revolutionize the IC Substrate and PCB Markets

Feature by Emilie Jolivet
YOLE DÉVELOPPEMENT

The smartphone is one of the high value-add products that carries a very high demand for miniaturization. Customers expect larger screens, cameras with high resolution, and various other functions, in lighter and thinner phones. In 2017, Apple requested a new "board," a substrate-like PCB (SLP), for iPhones. This has resulted in a technology transition for the PCB manufacturers and the need to invest in a modified semi-additive process (mSAP). New competitors were also attracted to this field: IC substrate manufacturers who originated the mSAP technology.

As a result, there were high capital expenditures among the SLP suppliers for Apple. This was followed by Samsung; the Galaxy S9, released in early 2018, has also adopted SLP technology, and similar high capital investments were made by some Korean PCB manufacturers. Additionally, increasingly more PCB and IC substrate manufacturers that were not in Apple and Samsung's supply chain are joining the competition of fabricating SLPs.

Starting with the adoption of SLP late in 2017, the volume is expected to grow from 27 million units in 2017 to 440 million units by 2023 with a CAGR of 59.4%. The SLP revenue in 2017 is estimated to be $190M and will grow to $1.4B in 2018, then $2.2B by 2023 with a CAGR of 51% [1].

The interest in decreasing the feature size for a smartphone board is due to the demand for thinner but more functional smartphones. With increasingly more functions added, along with larger screens, the power consumption becomes a critical point. In the volume of a smartphone, the battery takes up most of the space. As the feature sizes on the board decrease, more integration can be achieved in a

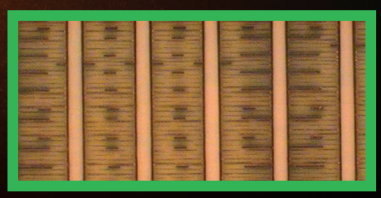
FILLING YOUR CHALLENGES ONE VIA AT A TIME

VIA FILL

BY TAIYO

THP-100 DX1 VF(HV)

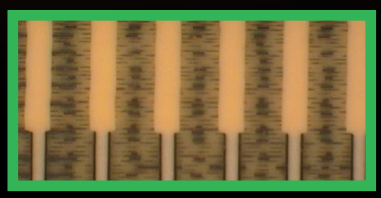
- Excellent Filling Characteristics for Large Holes
- 100% Solids, Low Shrinkage



THP-100 DX1 VF (HV)

THP-100 DX1 HTG

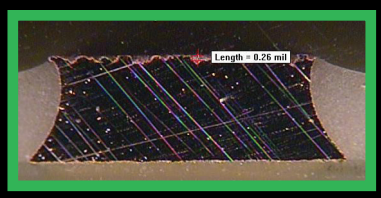
- Highest TG (173°C) Available on the Market
- Low CTE (19/55)



THP-100 DX1 (HTG)

THP-100 DX1 (GF) GAP FILLING MATERIAL

- Low Warpage
- Easy to Process



THP-100 DX1 (GF)

THP-100 (NEW VERSION)

- Short Curing Time
- Low CTE for Better Back Drilling

TAIYO AMERICA

Your Ultimate Solution

Phone [775] 885-9959 • www.taiyo-america.com • info@taiyo-america.com

fixed area. As can be seen in Figure 1, starting from iPhone 5s, Apple has gradually decreased the PCB area of the iPhones compared to the total smartphone area. Until the latest iPhone X, they have decreased 3% of the area while adding more functions and increasing the battery capacity. In the meantime, iPhone X not only adapted SLP but also stacked two SLPs like a sandwich to further increase integration in a fixed area.

This surface reduction was enabled by the increase of density and reduction of interconnection.

The semiconductor industry's trends are affecting the semiconductor package and package-to-board interconnect level. PCB traditionally serves as the interconnection of the chips and the final product, but nowadays it is also an integration solution. SLP is one of the answers today to the scaling demand while also responding to the functional roadmap.

SLP is so-named because this "board" has blurred the definition between a PCB and an IC substrate. Although usually fabricated by different technologies, the main difference between a PCB and an IC substrate is the feature sizes, especially line and space (L/S). Traditionally a PCB or even HDI board has feature sizes greater than 30/30 mm; an IC substrate, on the other hand, has L/S that is often >15/15 μm. Nevertheless, SLP has reached L/S that is smaller than 30/30 μm, and this has defined the name for SLP as it is a PCB that has the feature sizes close to that of an IC substrate.

Traditionally, PCBs are fabricated using a subtractive process that requires etching the pre-existing copper-clad laminate (>5 μm thickness). This often results in over-etching that cannot be compensated for afterwards. As a result, the minimum L/S using this technology is limited.

Different from the subtractive process, mSAP uses a negative pattern design to "grow" copper by electroplating on top of the pre-existing thin copper clad (<5 μm thickness, which serves only as the seed). Then the negative pattern is etched. mSAP is usually used for IC substrate fabrication and allows a further miniaturization of feature size for L/S. Until now, within the few smartphone models that have already adapted SLP, the L/S remains around 30/30 μm. However, the adaptation of mSAP for board is to further decrease L/S to increase

Apple Models	iPhone 5S	iPhone6	iPhone 6S	iPhone 7	iPhone 8	iPhone X
Flagship Model						
PCB Analyzed (System Plus Consulting) Main Board – Front Side)			Not Analyzed (considered pretty close to iPhone6)	Not Analyzed (considered pretty close to iPhone6)		
Phone Surface (mm^2)	7254.68	9252.7	9279.93	9279.93	9314.32	10181.24
Phone thickness (mm)	7.6	6.9	7.1	7.1	7.3	7.7
PCB Surface (mm^2)	1517.97	1834.73	1834.73	1834.73	1800	1849.2
Ratio (PCB area/.Phone area)	21%	20%	20%	20%	19%	18%
Technology	Subtractive	Subtractive	Subtractive	Subtractive	Subtractive + mSAP	Sandwich PCB Subtractive + mSAP

Figure 1: PCB analysis of Apple flagship smartphones.

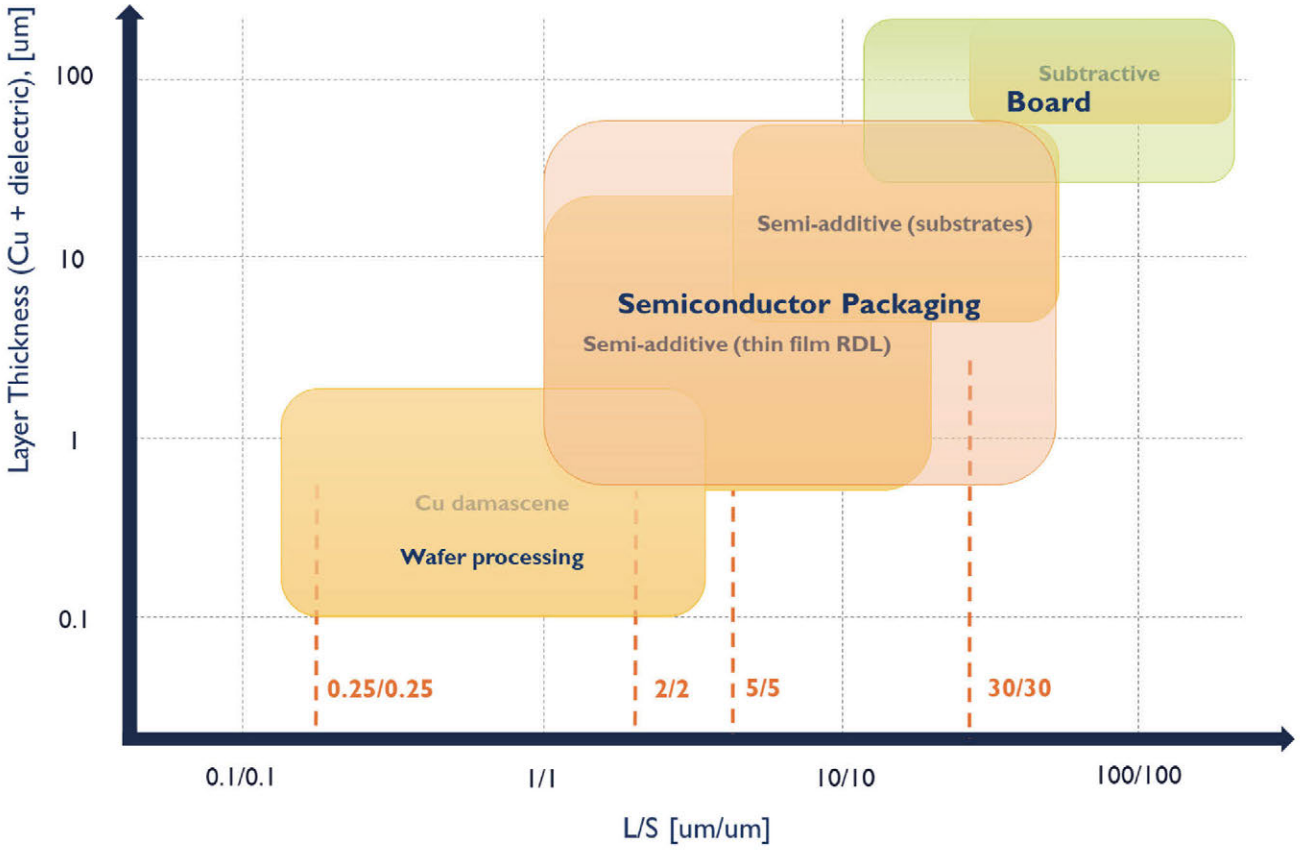


Figure 2: Advanced substrate technology segmentation projection.

integration. There are still challenges in adapting mSAP for board fabrication; current SLPs are not fully fabricated by mSAP but a mixture of subtractive and mSAP (Figure 2). Research and development is being done to gain more control of the fabrication process and further decrease feature sizes.

Figure 2 shows the vision of the advanced substrate technology segmentation regarding the demanded featured size. As can be seen, technologies that are traditionally used for different manufacturing steps start to overlap. SLP today gives an example of packaging technology used for board fabrication, in the future, other technologies will overlap as well and create potential new field of competition in the semiconductor industry.

Although only two smartphone manufacturers have adapted SLP to their flagship phones, it is expected that other large smartphone manufacturers such as Huawei, Xiaomi, and Vivo will follow this trend in the next few years. Smartphone manufacturers will continue the tendency of increasing integration in a fixed board area to add functions or to provide space for additional battery capacity. Other products that require strong miniaturization such as wearables, tablets, and tablet-PCs will most likely be the next products to adopt SLP.

While SLP is an answer to both scaling and functional demand today, there are more demands that need to be answered soon. The advanced substrate market will change dramatically compared to the past (Figure 3). The downsizing of board feature size and adoption of SLP will decrease the traditional PCB market; the evolving high-density fan-out (HDFO) technology along with downsizing of IC substrate will also decrease the IC substrate market. Although the market might increase slower in terms of volume, the added value of advanced substrates will keep increasing.

Today, the demand of scaling and function has strongly affected the semiconductor pack-

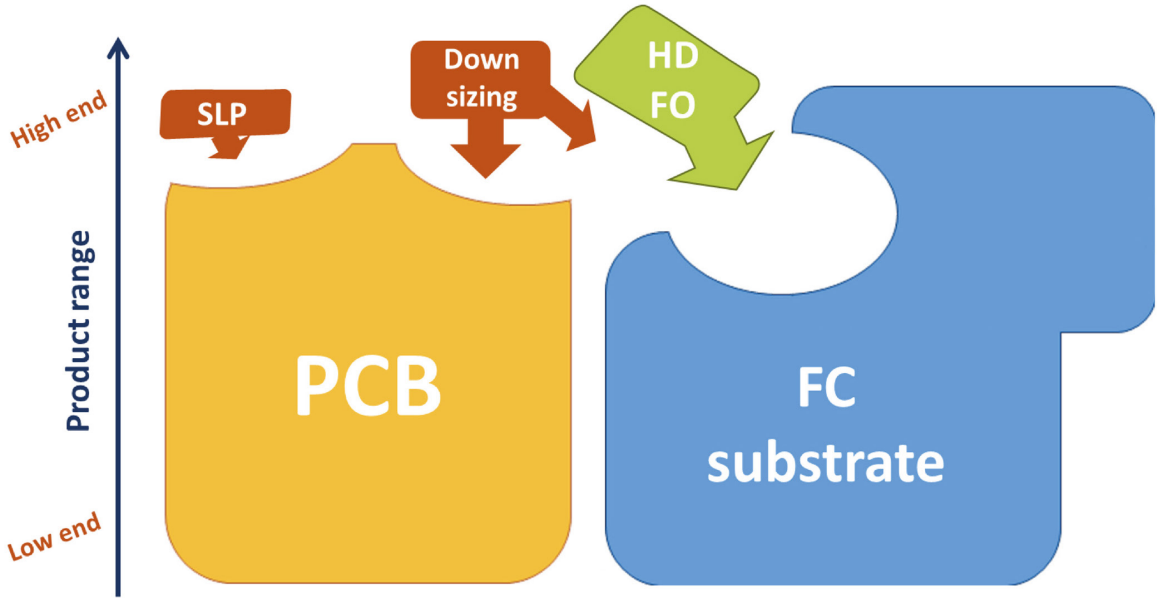


Figure 3: Advanced substrate market evolution.

aging technology and has provoked changes in PCBs. It became more than an interconnection but part of the integration of the package. The advanced substrate activity at Yole will keep on investigating these trends and provide more analysis of this market. PCB007

Images

All images from Yole Développement's report, "Status of Advanced Substrates: Embedded Dies & Interconnects, Substrate Like PCB Trends," February 2018.

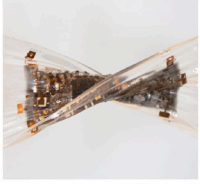
References

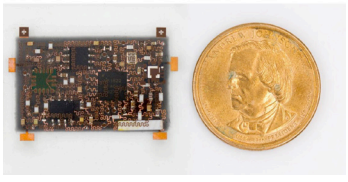
1. Status of Advanced Substrates 2018: Embedded Dies & Interconnects, Substrate-Like PCB Trends report, Yole Développement, February, 2018.

Emilie Jolivet is director of the Semiconductor & Software Division at Yole Développement, part of Yole Group of Companies, where her specific interests cover package and assembly, semiconductor manufacturing, memory, and software and computing fields.

'Building Up' Stretchable Electronics to be a Multipurpose Smartphone

By stacking and connecting layers of stretchable circuits on top of one another, engineers have developed an approach to build soft, pliable "3D stretchable electronics" that can pack a lot of functions while staying thin and small.





As a proof of concept, a team led by the University of California San Diego has built a stretchable electronic patch that can be worn on the skin like a bandage and used to wirelessly monitor a variety of physical and electrical signals, from respiration, to body motion, to temperature, to eye movement, to heart and brain activity.

"Our vision is to make 3D stretchable electronics that are as multifunctional and high-performing as today's rigid electronics," said senior author Sheng Xu, a professor in the Department of NanoEngineering and the Center for Wearable Sensors, both at the UC San Diego Jacobs School of Engineering.

(Source: UC San Diego)

GET YOUR 20% DISCOUNT!

WHEN YOU REGISTER BY ***12.21.2018***

APEX EXPO® IPC 2019

IPCAPEXEXPO.org
#IPCAPEXEXPO

SAN DIEGO CONVENTION CENTER, CA, USA

MEETINGS AND COURSES: *JANUARY 26–31, 2019*
CONFERENCE AND EXHIBITION: *JANUARY 29–31, 2019*

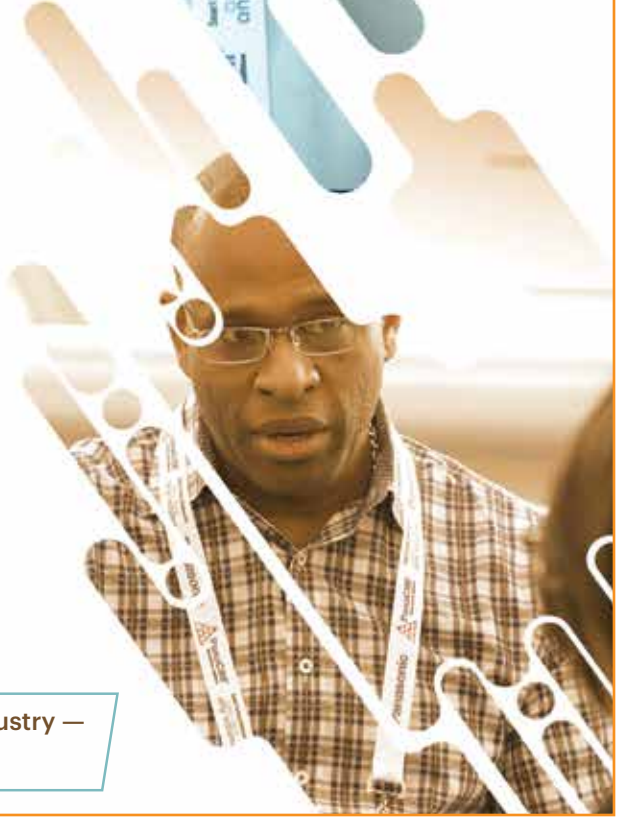
TECHNOLOGY'S FUTURE COMES TOGETHER

THROUGH NETWORKING

Technology's future will literally come together in San Diego at ***IPC APEX EXPO 2019*** on the exhibit show floor, in meetings, sessions and courses, and during networking events. The in-person exchange of ideas and know-how between you and your peers powers the industry's future.

Whether you are established in your career or just starting out, ***IPC APEX EXPO 2019*** will be the event to:

- Network with thousands of electronics industry peers
- Make new connections
- Strengthen existing relationships
- Become a mentor/meet a mentor



Strengthen the opportunities for yourself and the entire industry — register today for IPC APEX EXPO 2019 at ipcapexexpo.org.

Electronics Industry News and Market Highlights

Artificial Intelligence, Cloud Manufacturing, Internet Security, and Cyber Physical Systems Driving Industrial Innovations ▶

The growth of IoT has transformed the way end users interact with machines (automotive, home appliances, etc.). The manufacturing industry is expected to witness a digital revolution with advancement in hybrid sensors, predictive analytics, wearables, digital twins, mass customization, 3D printing, edge computing, robots, asset monitoring, smart grids, and natural processing language.

Artificial Intelligence Model 'Learns' from Patient Data to Make Cancer Treatment Less Toxic ▶

MIT researchers are employing novel machine-learning techniques to improve the quality of life for patients by reducing toxic chemotherapy and radiotherapy dosing for glioblastoma, the most aggressive form of brain cancer.

Growing Demand for Edge Computing in IoT ▶

The mobile AI market is expected to reach $17.83 billion by 2023 from $5.11 billion in 2018, at a CAGR of 28.41% during the forecast period.

Scientists Reduced the Weight of Optics for Satellite Observation of the Earth by 100 Times ▶

This optical element, created by the research group of the Department of Supercomputers and General Informatics of Samara University, weighs only five grams and replaces a complex and massive system of lenses and mirrors similar to the one that is used in telephoto lenses with a focal length of 300 mm and a weight of 500 grams.

3D Printing the Next Generation of Batteries ▶

Additive manufacturing, otherwise known as 3D printing, can be used to manufacture porous electrodes for lithium-ion batteries—but because of the nature of the manufacturing process, the design of these 3D printed electrodes is limited to just a few possible architectures.

Sensor Technology to Improve Safety and Health in Aged Care ▶

Flexible sensors developed at RMIT will be integrated into new health monitoring technology to improve aged care, in a project supported through a $1.7 million Federal Government grant.

SEMI Testifies Against U.S. Tariffs, Members Meet with Congressional Leaders Urging Trade Action ▶

Two months after opposing $34 billion in U.S. trade tariffs on behalf of the U.S. semiconductor manufacturing industry, Jonathan Davis, global vice president of industry advocacy at SEMI, this week spoke out against an additional $16 billion in duties on Chinese goods.

New 3D-Printed Device Could Help Treat Spinal Cord Injuries ▶

Engineers and medical researchers at the University of Minnesota have teamed up to create a groundbreaking 3D-printed device that could someday help patients with long-term spinal cord injuries regain some function.

Semiconductor Market in Military and Aerospace Industry 2018-2022 ▶

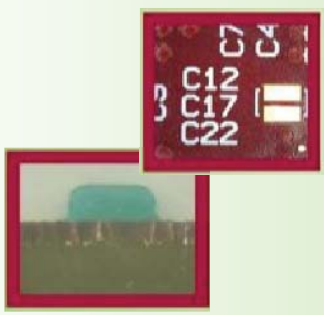
The Global semiconductor market in military and aerospace industry to grow at a CAGR of 7.53% during the period 2018-2022.

MivaTek Global

MIVA TECHNOLOGIES

LED Direct Imagers

Most flexible system
Most diverse customer base



- **Inner Layer:** 10, 25, and 50µ features
- **Outer Layer:** Incredible scale accuracy
- **Soldermask:** 2 mil solder dams, MDP capable
- **Legend Ink:** Excellent resolution for inkjet backup

- **Photoresists:** Any available on the market
- **Soldermasks:** Any available color

- **Factory Support:** Throughout North America

MIVA: LED DIRECT IMAGING

NEW PRODUCTS NOW AVAILABLE

3000LS Large Area Direct Imager

- 30" x 60" standard imaging area
- 1 mil registration accuracy (A/B)
- Up to 3 light engines for high throughput
- Small footprint for the imaging area
- 10, 25 and 50µ feature systems available
- Images all materials resist and soldermask

2400L Dual Tray Direct Imager

- Simultaneous panel loading and imaging
- Automation available from third party sources
- High efficiency systems for all applications
- World class Miva Direct Imaging technology
- 10, 25 and 50µ feature systems available
- Configurations for 30 to 120 panels per hour

NEW PRODUCTS

MivaTek Global, 6 Dickinson Drive, Suite 215, Chadds Ford, PA 19317
Eastern US: Brendan F. Hogan, M (610) 620-3795, B.Hogan@MivaTek.Global
Western US: Kurt Weber, M (714) 767-6367, Kurt@MivaTek.Global

Understanding Resist Lock-in and Extraneous Copper

Trouble in Your Tank

by Michael Carano, RBP CHEMICAL TECHNOLOGY

It happens when you least expect it. You think you have all the process controls in place to prevent issues after etching, but either copper remains where there should be none or photoresist remains on the copper. Regardless, it is a problem and must be fixed; what are some of the causes?

Resist lock-in comes in many shapes and sizes. Figure 1 shows an example of extraneous copper. The root cause of the remaining copper is often resist lock-in.

In addition, several causes for the extraneous copper defect can be attributed to:

- Excessive resist lamination temperatures: This can cause thermal cure of some photoresists and difficulties in developing cleanly
- Oxidation of the panels prior to resist lamination
- Wet lamination: A thin layer of water is applied to the copper surface prior to resist lamination and requires resists that are compatible with wet lamination in order to avoid resist lock-in, which will lead to excess copper. According to Dr. Karl Dietz, one must strictly adhere to hold time and its conditions

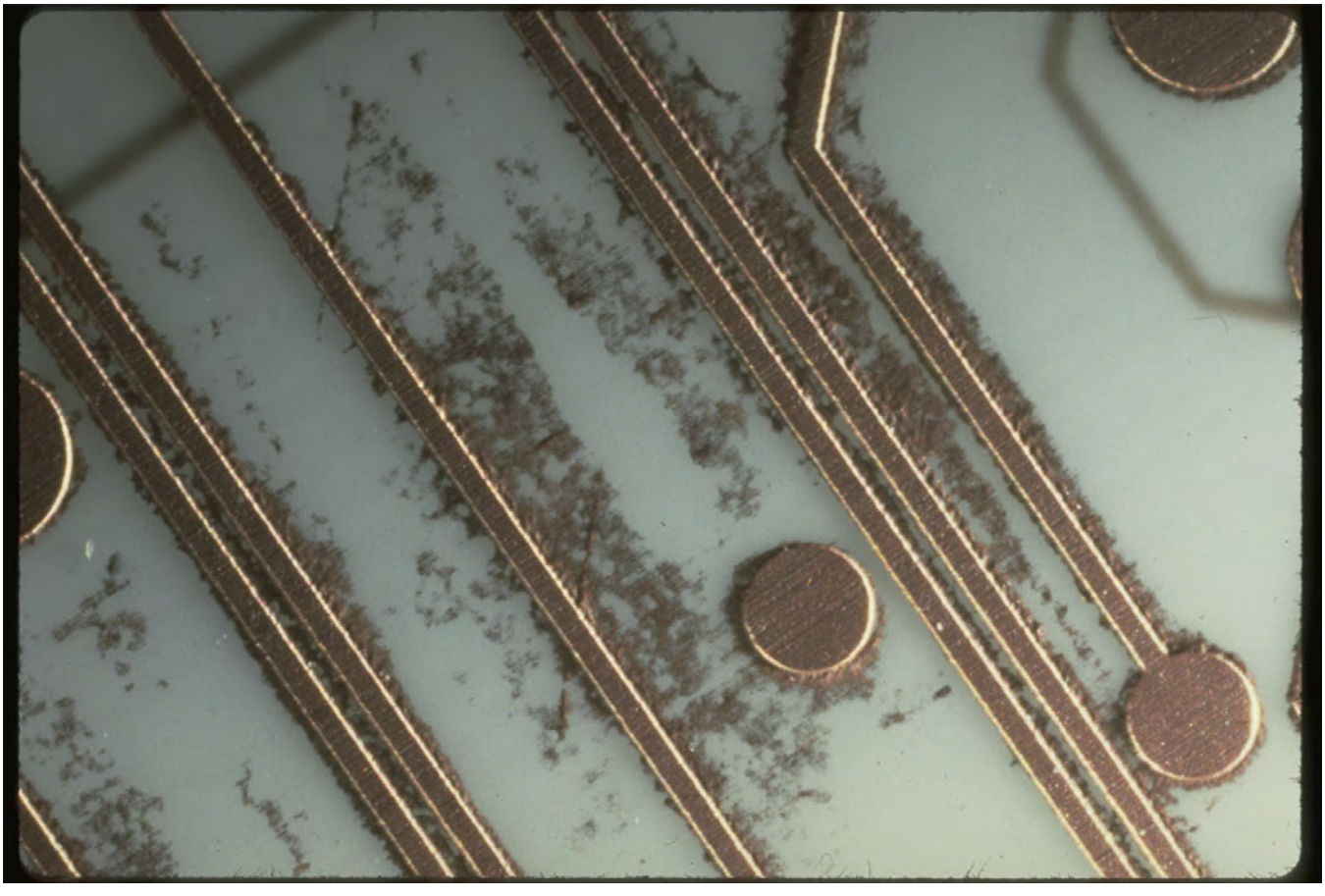


Figure 1: Extraneous copper.

Get HyperLynx DRC for FREE for 12 months

COMPATIBLE WITH ANY PCB LAYOUT TOOL!

www.mentor.com/get-drc

visit us at SMTA International booth 933

- Dry lamination issues: This holds especially true if the post-lamination hold time is too long or temperature and humidity are too high during hold time. Such conditions favor copper oxidation. In terms of oxidation, there will be a strong tendency for the laminated resist to strongly adhere
- Exposure of the copper surface to hydrochloric acid fumes: This may cause resist lock-in even if post-lamination hold times and conditions are normal. As in often the case, the resist-laminated panels for inner-layer processing may contact acid fumes from the cupric chloride etching process
- Excessive pressure on the hot roll laminators or too high a temperature
- Excessive surface roughness (topography) due to overly aggressive chemical cleaning or scrubbing of the copper surface: If you suspect lock-in due to a non-uniform or over-roughened surface, a profilometry study to measure surface roughness might be in order
- Developer/unexposed resist residues remaining on the copper surface in a random fashion: This happens due to insufficient rinsing or inadequate control of the developing solution. In the latter case, the main culprit is too low a pH in the developer solution. Another cause is partially polymerized resist that was not completely developed away

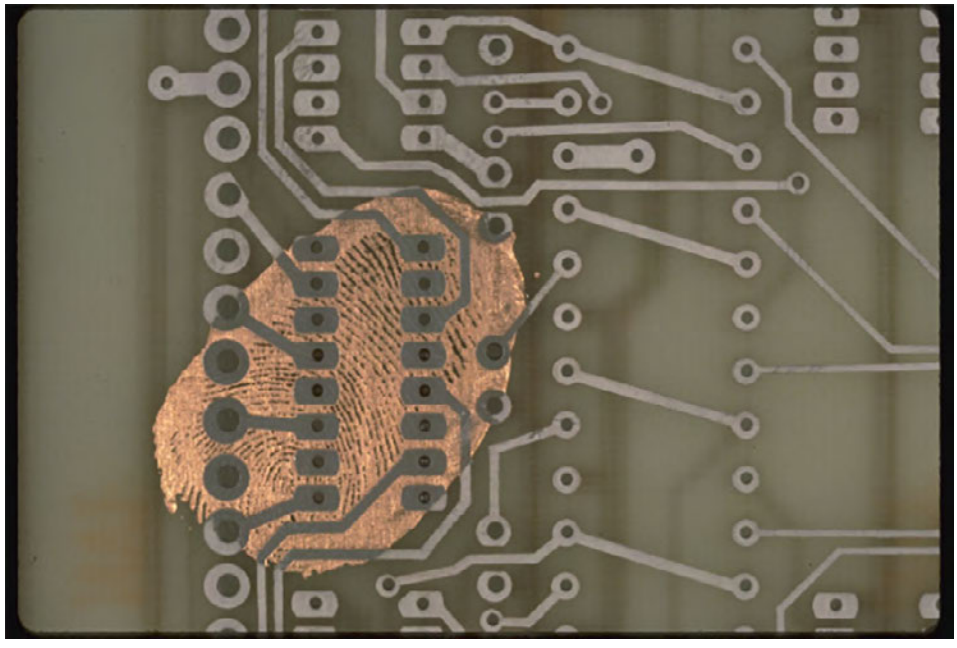


Figure 2: Copper not removed due to a fingerprint from poor handling.

Of course, extraneous copper can sometimes be linked to obvious causes, but that does not make it any less frustrating (Figure 2). While improper handling is somewhat of a rare occurrence compared to other issues, this must be considered. For example, did the operators wear gloves? It would be a major mistake to think strong cleaners will remove human fingerprints, so tread cautiously.

Surface cleanliness is critical to ensure photoresist adhesion. In addition, topography provides a mechanism to enhance adhesion of the resist to the copper surface. However, the critical aspect is to have an overall roughness of the surface area that is uniform and not overly roughened with chemical etchants or mechanical means. A surface that has major deviations from peak to valley along the surface profile will adversely affect resist adhesion. Thus, there is the potential for lock-in on one extreme and resist lifting on the other.

Best practice dictates diligence with surface preparation, resist lamination, hold times between process steps (in-process is best due to minimal holds), and all processes associated with the resist exposure and development. **PCB007**

Michael Carano is VP of technology and business development for RBP Chemical Technology. To read past columns or contact Carano, click here.


Meet your new sales personal trainer.
Increasing sales isn't rocket science. We use proven methods to help you find the right customer, motivate your sales team, and increase your profits.
We've helped dozens of companies big and small improve their bottom line.
Learn how we can help YOU
db MANAGEMENT GROUP
207-649-0879
danbbeaulieu@aol.com

Copper Pillar Plating Systems: High Speed, Low Heat

Article by E. Walch, DJ., C. Rietmann, Ph.D., and A. Angstenberger, Ph.D.
MACDERMID ENTHONE ELECTRONIC SOLUTIONS

Abstract

The industry is seeing ever-more stringent requirements of interconnect technologies (ICT) from die through final assembly, in particular digital and analog high frequencies, undistorted signal propagation and efficient heat propagation are concerned. From wafer level packaging to the finished printed circuit board, copper pillars, and solid copper posts (with printed circuitry it is copper filled through-holes, respectively) continue to play a vital role in coping with high-speed/high-frequency and high wattage of sub and final assemblies.

Commonly used packaging concepts comprising wafer level plating, through-silicon-vias (TSV), redistribution layer design (RDL), intermediate pillars, macrobumps and copper-filled through-holes in the final circuitry will be addressed in this article, followed by an overlook of the extremely different pillar geometries within each packaging level, posing individual challenges on the copper plating chemistry and process. Practical aspects, namely dialing in the chemistry additives and process windows to match the relevant applications' needs will be reported, as well as the ongoing R&D work targeted for current and future requirements. The article concludes with actual research results on achievable copper textures and the subsequent performance of the plated copper interconnects as far as crystal lattices and the related thermal reliability are concerned.

Introduction

Chasing the Speed-Coping with Heat

Stunning die architectures and thus the ubiquitous subsequent miniaturization throughout any overall electronic assembly continue to gather momentum on the basic current and future challenges on interconnect technology (ICT) namely:

- Signal (analog and digital) frequencies up to 100 GHz, even beyond
- Heat generation up to 150 W/cm^2
- Utilization of 3D structures (component stacks)

BÜRKLE

NORTH AMERICA, INC.

LAMINATION SYSTEMS FOR PRINTED CIRCUIT BOARDS

STATE-OF-THE-ART SOLUTIONS FOR THE PCB INDUSTRY INCORPORATING THE LATEST TECHNOLOGY.

Solutions for the PCB Industry

High quality and well proven presses and handling equipment

INNOVATIVE POWER **4U**

Contact:
Dave Howard
714-379-5090

burkleamerica.com

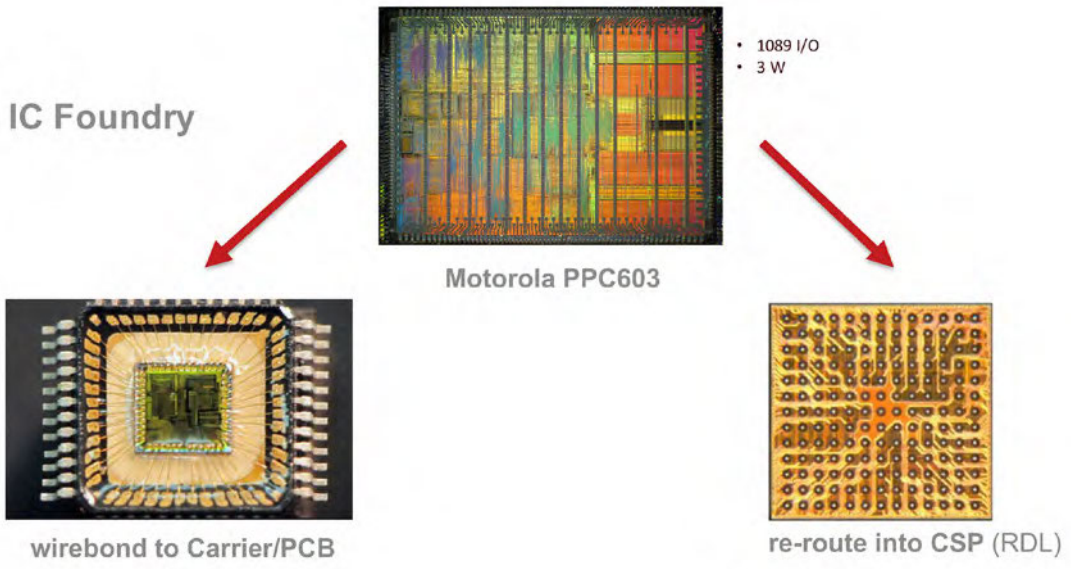


Figure 1: Wirebond and redistribution scheme.

- Mitigation of conductor parasitics (straight metal connects vs. wirebonds)
- Effective heat paths leading from single "hot" components through the assembly to the environment

Starting from the integrated circuit (IC) foundry, the first packaging step would be either wire-bonding a naked die to a carrier/PCB or re-routing the die-pads (I/Os) into a chip-size- or chip-scale package (CSP) utilizing one side of a die as a redistribution layer (RDL). Any carrier (aka, interposer) as well as CSP may be fitted with connecting metal studs, pillars, and bumps, thus providing the option for 2.5D or 3D stacking, not to mention the final soldering of ball grid arrays (BGAs) to a printed circuit.

For ease of illustration and clarity any (repeated) three-dimensional "component" stacking procedures are intentionally left off in Figure 1.

Figure 2 shows the subsequent packaging steps onto carriers prior to component soldering to the PCB.

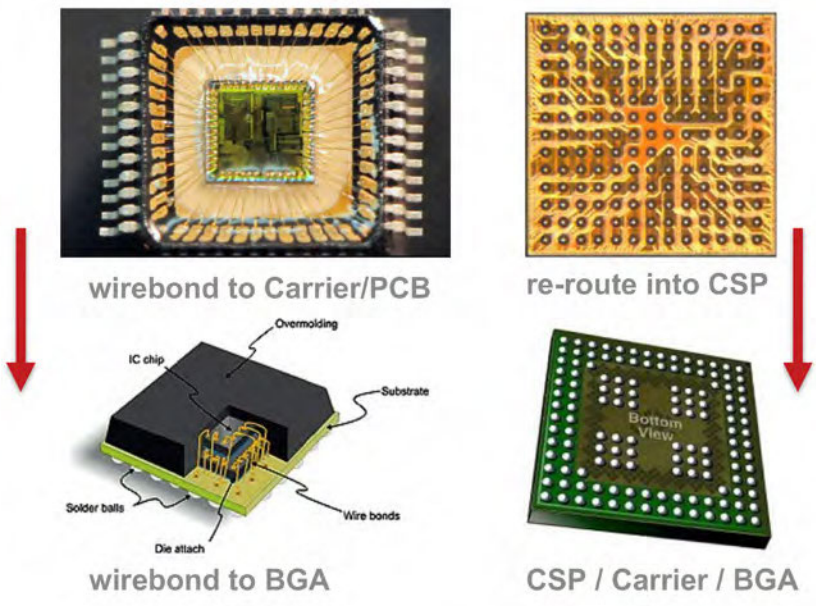


Figure 2: Stepping forward to subsequent soldering onto printed circuits.

Packaging Level	Measure for Heat Conduction	Thermal Conductivity Z-axis
wirebonded dies	thermal adhesives, metal core/ backed substrates	5–10 W/mK
CSP (~stacked)	designed in thermal/GND pads, copper studs, pillars, bumps	Up to 390 W/mK
BGA carrier, interposer, substrate (silicon, glass, organic)	thermal vias, thermal THs, copper filled metal core/backed substrates	Up to 390 W/mK 5–10 W/mK
PCB	thermal vias , thermal THs , copper filled metal core / backed substrates	Up to 390 W/mK 5–10 W/mK

Table 1: Various measures of heat dissipation at various packaging levels.

An example of a full 3D stackup will be presented later. Table 1 represents schematically the possible measures to effectively dissipate the heat (i.e., conducting the excessive power from any die through the various packaging steps to the environment).

Thus utilizing (already designed-in) thermal/GND pads on silicon may provide a seamless and most effective heat path from die through the final assembly on a printed circuit board—if the interconnects on each packaging level are performed by copper studs, pillars, bumps—thermal vias and through-holes filled with copper on PCB level respectively.

Besides any heat dissipation effects said copper studs, pillars, bumps, copper-filled thermal vias and through-holes do provide the shortest, extremely reliable, least parasitics-afflicted electrical interconnects.

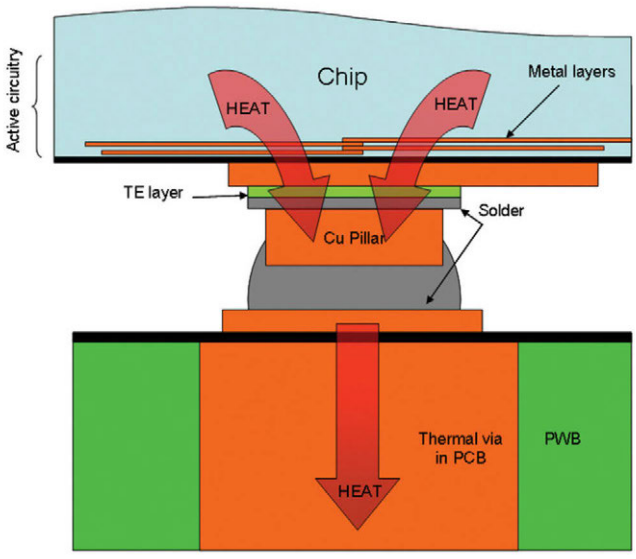


Figure 3: Forced heatflow by Peltier elements. (Source: Nextreme)

As being depicted in Figure 3, advanced die designs even utilize forced heatflow practises (e.g., Peltier effect) to additionally cool down hot chips through copper and solder interconnects—again, copper filled vias and/ or through-holes become mandatory for utmost thermal effectivity.

For clarity of demonstration Figure 3 shows only one of the needed P-layer/N-layer twin pillars needed for driving the Peltier effect.

Figure 4 illustrates the breathtaking complexity of a smartphone processor package—even several mobile phone generations back.

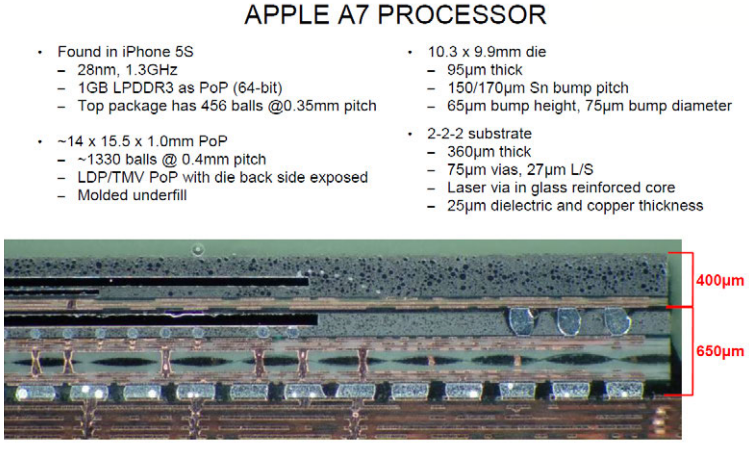


Figure 4: From die through environment–full packaging complexity. (Source: Prismark/Binghamton University)

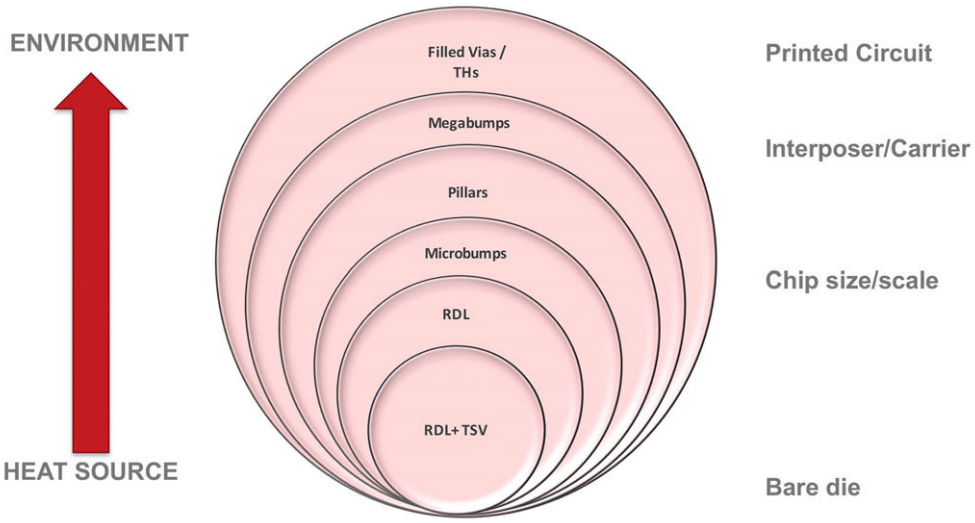


Figure 5: The seamless speedy copper path.

From Foundry through Assembly

Providing a seamless electrical and thermal path from bare die to the final assembly´s environment already starts with the design of an integrated circuit and continues by designing in high-performing bumps, pillars, studs, and vias subsequently on interposers, carriers, substrates, and printed circuit boards (Figure 5).

At each design stage, extremely different circuit and interconnect dimensions—application specific—do apply, ranging from µm to mm values (Table 2). These far spanned geometries—visualized in Figure 6—do require different electrolytes, different process conditions, and carefully adjusted equipment (tools) for copper plating pillars, studs, bumps, and filled vias/through-holes.

Geometry and Chemistry

The already cited various and extremely different geometries simultaneously have specific requirements on performance, namely:

- Coplanarity (current density, feature density, etc.)
- Bump shape modulation (chemistry selection, bump opening)

And, as always, everyone´s target on cost reduction is impacted by:

- Plating speed: from 2-4 µm/min and beyond
- Bath life: Photoresist compatibility, additives´ by-products

Feature	Plating attributes	Diameter, L/S	Height	Package	Feature on	Application
RDL	Coplanarity, L/S tolerance	1.5 µm / 1.5 µm	<2 µm	Fan-Out	Wafer	Memory + AP / baseband
Micro bump	Coplanarity , KV free	<30 µm	<20 µm	2.5D & 3D IC	Wafer	HMC, FPGA
Cu pillar	Coplanarity , speed	30 - 60 µm	30 - 50 µm	FC & 2.5D	Wafer	CPU, APU, baseband, DDR4 SDRAM
Cu pillar	Coplanarity , speed	60 - 80 µm	50 - 70 µm	FC & 2.5D	Wafer	Power amplifier
Large bump	Speed	90 - 110 µm	40 - 60 µm	FC & 2.5D	Wafer	FPGA
High Cu Pillar	Coplanarity , speed	110 - 200 µm	130 - 180 µm	PoP	Substrate	Memory + AP / baseband
Mega bump	Speed	200 µm	200 µm	3D fan out	Wafer	Memory + AP / baseband
Via / TH fill	Dimple, surface thk, speed	75 - 400 µm	< 0.8 mm	Assembly	Carrier / PCB	Unlimited
3 in 1	All of the above	Full range		Multiple	Wafer	Mobile

Table 2: Typical dimensions and applications along the interconnect seam.

Ucamco
Former Barco ETS

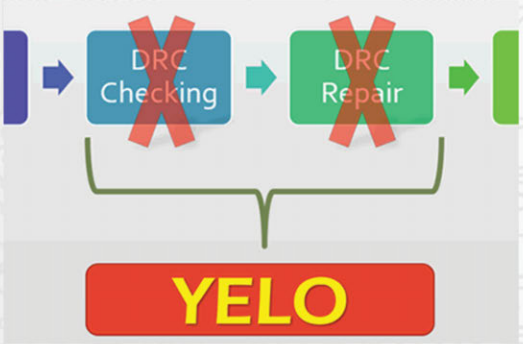
SOFTWARE | PHOTOPLOTTERS | DIRECT IMAGERS | NEWS | SERVICES | COMPANY | DOWNLOADS | CONTACT

Software

YELO

Yield Enhancing Layout Optimizer

- Optimizes board layouts within minutes
- Cuts back CAM cycle time & cost by up to 30%
- Lowers technology class improving manufacturability
- Reduces scrap and delivers a more reliable product
- Return on Investment within the first year



Read more

Need a Gerber Viewer?

Ucamco, caretaker of the Gerber format, presents its new Reference Gerber Viewer. Use this free online tool to view and/or check your generated/received Gerber jobs.

- Reads X2 attributes containing PCB fabrication data
- Imports Excellon and NC drill files

Go ahead and link your site to https://gerber.ucamco.com

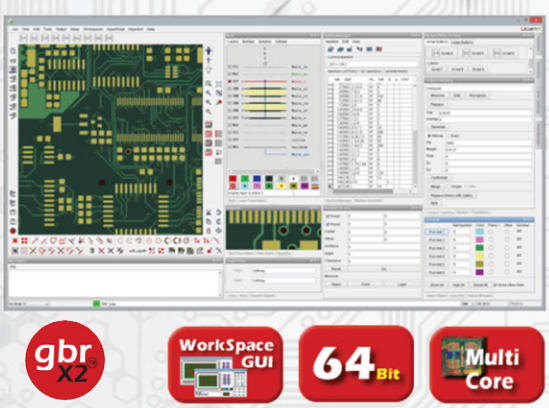
Software

UcamX

New ground-breaking CAM Software

- For Rigid, Flex and HDI PCBs
- New Graphical User Interface with Workspaces
- Optimal performance using Parallel Processing
- Multi Job Processing via load balanced Sessions
- Support for Gerber version 2 (X2) format

Read more



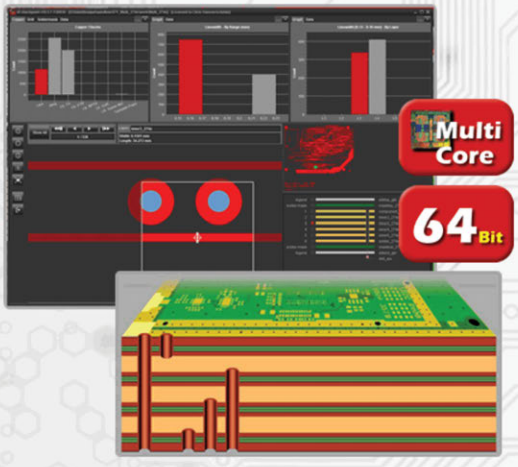
Software

Integr8tor

Automated data entry and design analysis

- Ucamco's 9th Generation Sales & Engineering Tool
- Field proven with more than 300 installations in daily production
- Seamless integration into any environment

Read more



For more information please contact info@ucamco.us,
call (415) 508-5826 or check out our website at www.ucamco.com

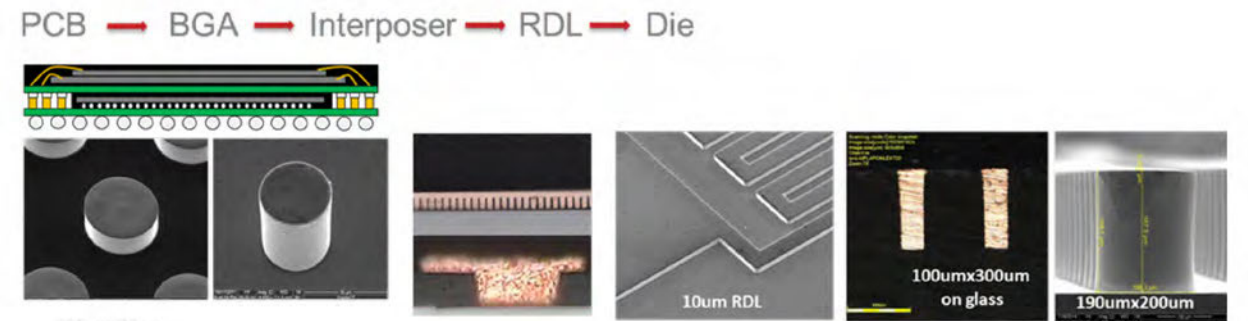


Figure 6: Different geometries requiring different chemistry/process parameters/tools for copper plating.

Table 3 summarizes critical attributes and the various bump shapes that are application specific.

It has to be stated that a one-fits-all application chemistry and its needed equipment configuration will be hard to find, if at all. Before diving into the depth of copper pillar technologies and the related development routines, a closer look at the generic hydrodynamics of any pillar feature during electroplating/filling is shown in Figure 7.

Developing the adequate plating chemistry (additives, basic concentrations copper/sulfuric acid/chloride) with respect to plating current

Applications	Critical Plating Attribute	Bump Shape
RDL	Coplanarity	Flat to domed on flat substrate
Micro bumps	Coplanarity	Flat on passivation substrates, domed on flat substrates
Cu Pillars	Coplanarity at high speed (≥3.5 mm/min)	Flat on passivation substrates, domed on flat substrates
Macro bumps	Bump shape control & speed	Flat to domed on passivation substrates
Mega bumps	Coplanarity, very high speed (>6 mm/min)	Flat to dished, to slightly domed on flat substrates
Filled via / TH	"Post" shape control & speed	Flat to dished, low surface copper

Table 3: Critical attributes/bump shapes for various plating applications.

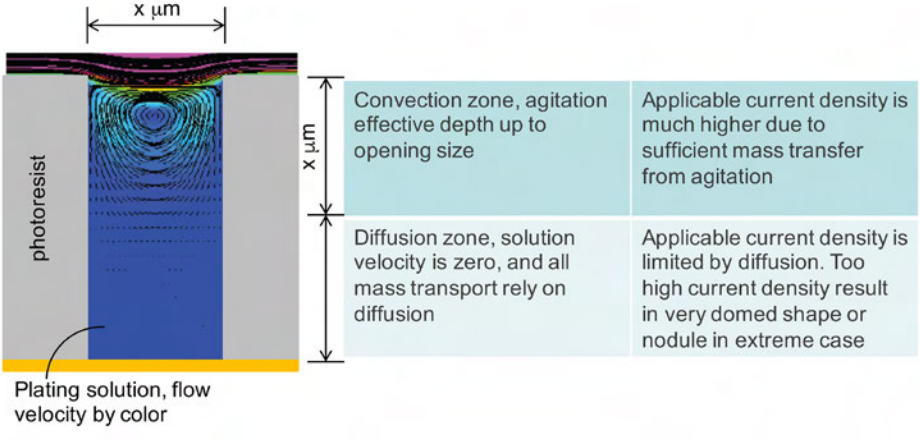


Figure 7: Diffusion zone and limiting current govern any pillar copper plating. (Source: AMAT, Kalispell MT)

WHAT DO ALL OF THESE LEADING COMPANIES HAVE IN COMMON?

ATOTECH

CIMS
Creativity in Motion

Cerambus
Technology Group

COMETGROUP
Technology with Passion

DownStream
Technologies

esi
Designed for Brilliance. Engineered for Production.

KIC Making Ovens Smarter™

KYZEN

MacDermid Enthone
ELECTRONICS SOLUTIONS

Mentor
A Siemens Business

PULSONIX

orbotech
The Language of Electronics

ventec
INTERNATIONAL GROUP
騰輝電子

環球集團
World Wide Group

They all benefit by advertising with us–PCB007 China Magazine.

Should your name be on the leaders' list?

GET STARTED NOW!

I·Connect007
GOOD FOR THE INDUSTRY

pcb007china.com

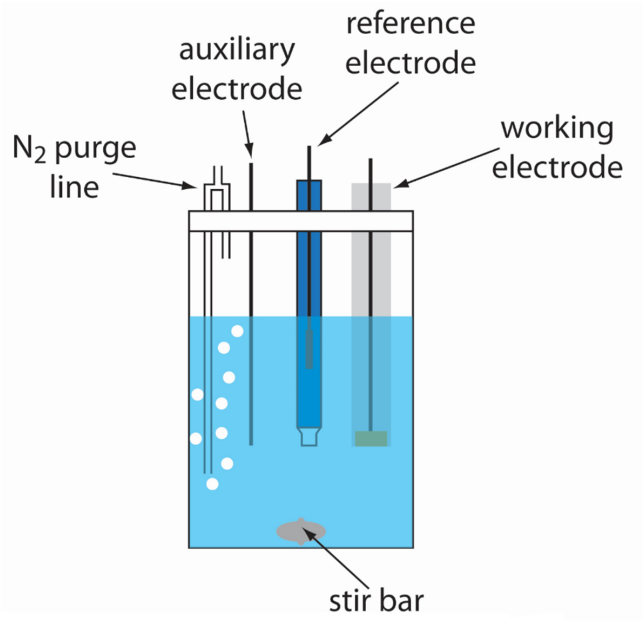


Figure 8: Schematic of a voltammeter.

density and plating equipment (hydrodynamics) is basically being performed for any type of interconnect geometry (µm to mm range) by using voltammetry and/or chronopotentiometry as the most powerful tool for any start-up qualification (Figure 8).

Typical state-of-the-art basic copper electrolytes (e.g., virginal makeup solution or VMS) consist of copper sulfate, sulfuric acid, plus chloride ion; the latter may also be regarded as an accelerating active additive controlling the lattice and grain buildup of the electroplated copper. Concentrations in a particular VMS need to be adjusted to any geometry's requirements; they govern the magnitude of the limiting current and thus the final plating speed as well as the geometrical perfection of the needed copper feature.

The Butler-Volmer-based equation applies:

$$i_{limiting} = \frac{nFD}{\delta} C^*$$

n = Ion charge
F = Faraday constant
D = Diffusion coefficient
C* = Ion concentration
δ = thk diffusion layer

Typical additives—influencing lattice geometries—to a VMS are suppressors (wetting copper surfaces, controlling diffusion), activators (refining grain sizes by proliferation of nuclei) and so-called levellers caring for feature uniformity, feature shape (Table 4). Details of Kirkendall-void aspects will be presented later in this article.

For any particular copper feature/geometry the best suited leveller—in concert with the other bath constituents and additives (Table 4)—needs to be designed to its best molecular constitution and qualified by said electrochemical methods.

The achievable throwing power (i.e., degree of uniformity of the macroscopic current distribution) can be predicted and application specific characterized by the Wagner number W_a:

$$W_a = \frac{\text{activation resistance}}{\text{ohmic resistance}} = \frac{R_a}{R_\Omega} = \frac{\kappa}{\ell}\left(\frac{\partial \eta_a}{\partial i}\right) = \frac{\kappa}{\ell}\frac{\beta}{i}$$

κ = electrolyte conductivity
l = distance between anode and cathode
β = Tafel slope

Attributes	Electrochemistry	Primary control	Secondary control
Bump height uniformity	High Tafel slope (W_a)	Leveller	H^+, current density, temp, Cl^-
Flat bump shape	Minimal difference in polarization between high and low agitation (Δ E)	Leveller and suppressor	Cu^{2+}, Cl^-, agitation

Table 4: Bath constituents controlling feature attributes.

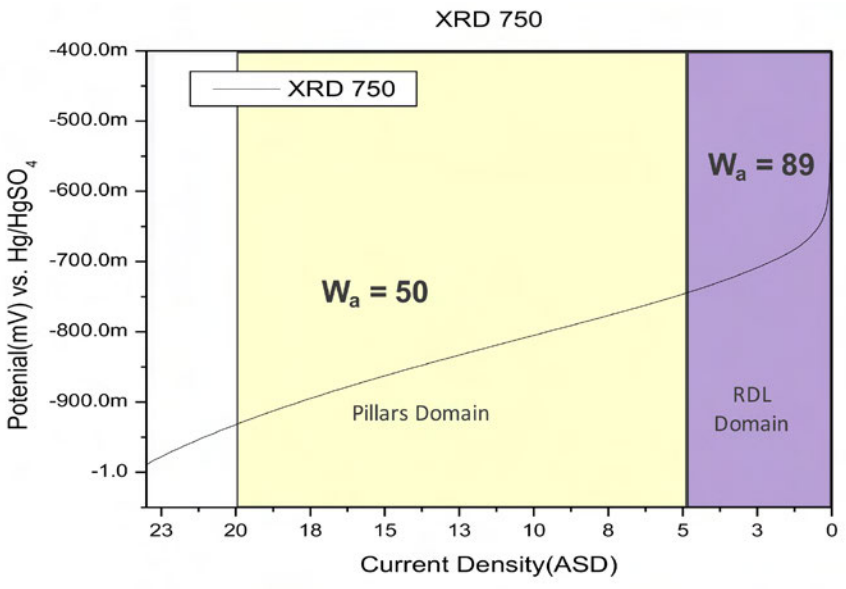


Figure 9: Characterizing designed levellers by voltammetry.

W_a and its mathematical predecessor, the Tafel slope b, both basically represent the slope in the potential/current diagram of a given electrolyte and control in the end the domain where a leveller can be successfully applied (Figure 9).

When designing and synthesizing new leveller compounds, chronopotentiometry (Figure 10) allows for rapid characterization and—much more importantly—a reliable prediction of the bottom-up-fill capability (go or no-go discrimination). Needless to mention, a VMS suitable for the relevant geometry/copper feature has already been composed.

Any leveller reducing the electrochemical potential at high agitation as compared to low agitation will be basically suited for bottom-up fill because of "directing" the plating current into the feature to be filled (i.e., preferential deposition at low current density areas).

Dialing in the Application

Once the VMS has been chosen for and the needed/suited additives have been designed and prequalified, the subsequent task is now to determine the optimum concentrations of brightener, leveller and carrier.

Figure 11 shows an example of a leveller´s characteristic. Its growing concentration does not impact the limiting current but considerably influences the bump/pillar uniformity—in particular within die (WID) and within feature (WIF) numbers of bump heights.

Again, different bath concentrations yield different polarographs and need to be dialed into the envisaged plating tool and the

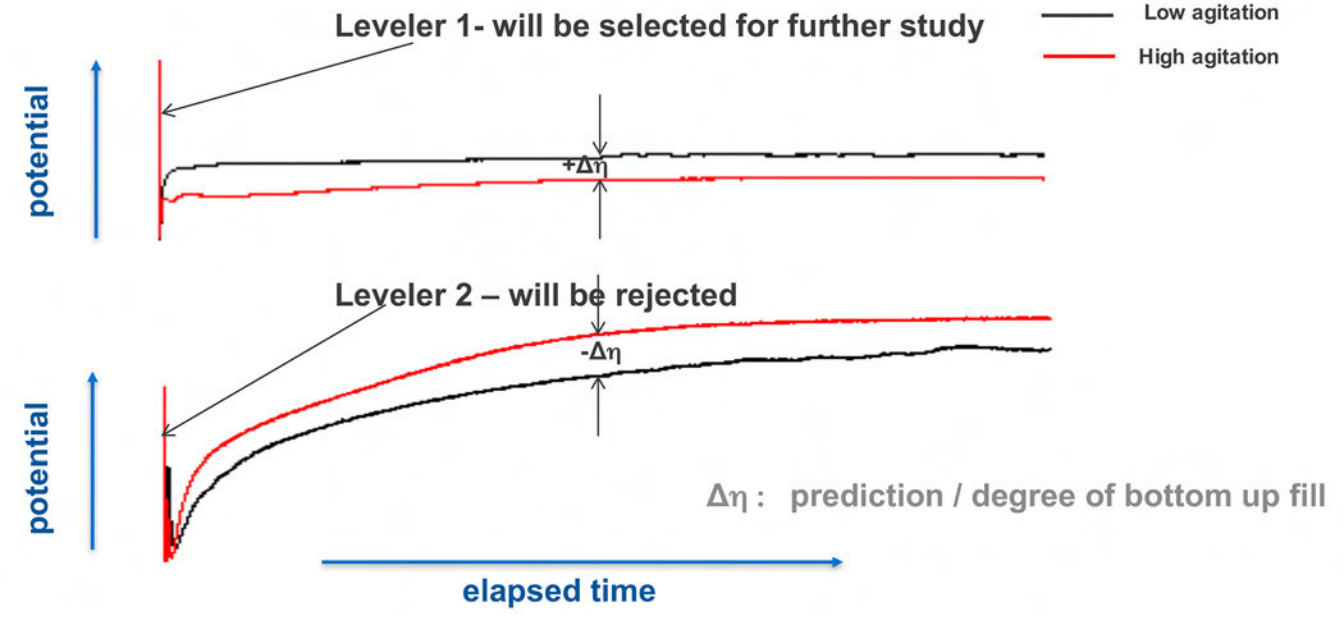


Figure 10: Leveller selection and qualification (chronopotentiometry).

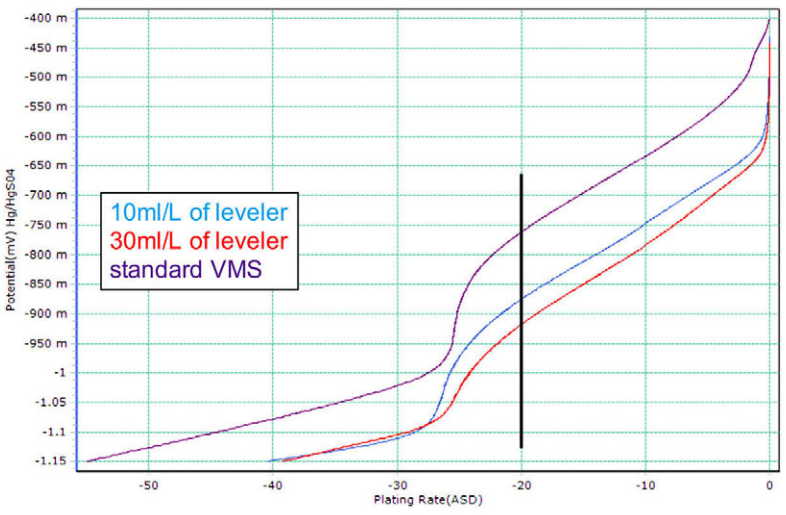


Figure 11: Leveller concentration and limiting current.

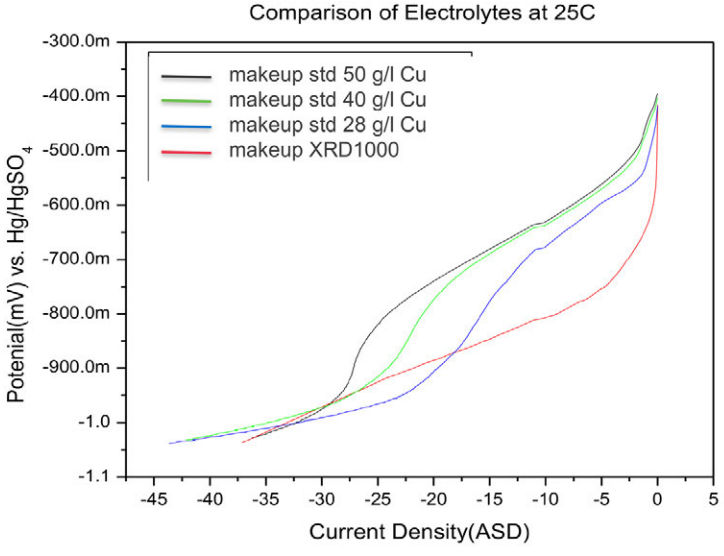


Figure 12: Application-specific bath-type selection.

Process	[Cu] g/L	Accelerator	Suppressor	Leveler
Mega bumps	80-90	Strong	Strong	Strong
Pillars	40-50	Strong	Weak-Strong	Strong
Micro bumps	10-30	Strong	Strong	Weak
RDL	10-20	Strong	Strong	Weak-Strong
RDL + TSV	40-50	Weak	Weak-Strong	Weak-Strong

Table 5: Dialing in the application.

planned application (TSV, RDL, pillars, bumps, filled through-holes), not to mention the optimum flooding and the best substrate agitation (Figure 12).

The terms "strong," "weak," and "weak to strong," stand for any additive's relative magnitude of its accelerating, suppressing, levelling power.

At the end of the day, it is not only the voltammetry/chronopotentiometry helping to design and qualify any particular chemistry for a given application/geometry/tool, but exhaustive designed experiments regarding:

- Chemistry/concentrations
- Current density
- Temperature
- Tool selection
- Tool auxiliaries

Therefore, a one-fits-all bath composition may still be a mere vision.

Typical electrochemical criteria for copperplating, in terms of activity of the single components, are listed in Table 5.

Copper Textures and Performance

Out of the manifold of possible copper lattices, the configuration as being named 1,1,1—per Bravais classification/Miller Indices—has proven to be the most preferred when speaking in terms of hardness and elongation and therefore reliability (Figure 13).

When flawlessly packed to each other, these basic bi-pyramidal cells build up to so-called nano-twinned columnar structures[1] being almost insensitive to the formation of Kirkendall voids[2-6] in intermetalic solder layers.

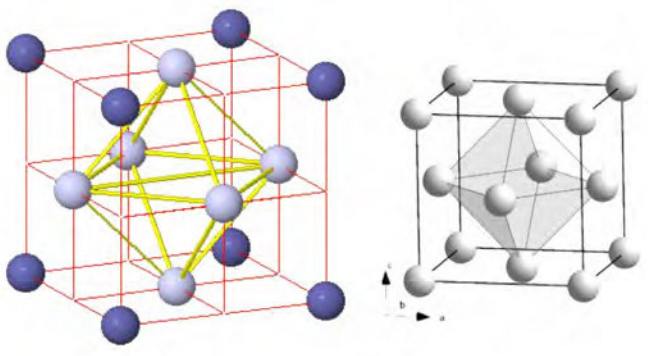


Figure 13: Always preferred–the 1,1,1 copper lattice.

Void generation happens in a two-way direction: Vacancies move towards the copper substrate and copper ions diffuse in the opposite way—10X faster than tin does, particularly in soldering. The relevant thermodynamics governing the void formation are shown in Figure 14.

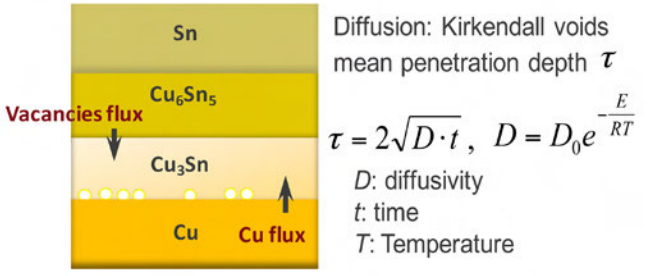


Figure 14: Thermodynamics of Kirkendall formation.

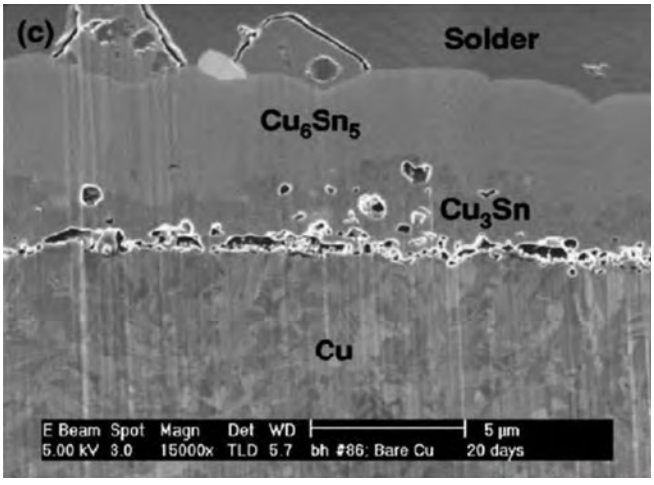


Figure 15: Kirkendall voids in intermetallic solder layers. (Source: K. Zeng et al., 2005)

The same factors cited above foster a perfect 1,1,1 copper cell unit being resistant to Kirkendall void generation:

- Chemistry/conc. (additives per se)
- Current density
- Temperature
- Tool selection
- Tool auxiliaries

The worst case scenario in Figure 15 has been deliberately chosen for.

Naturally, any given impurities (e.g., carbon-based, by-products, any contaminants) may lead to lattice distortions/defects as well thus preventing a flawless 1,1,1 copper cell formation.

The Macro PCB Section: Via Fill and Through-hole plating[7,8]

Figure 16 shows a perfectly filled blind microvia (BMV, size 5 x 3 mils) and a simultaneously copper plated through-hole (diameter = 8 mils).

The development and engineering work uses the same routines as for macropillars, as already described. For reasons of final qualification, the solid copper post in the BMV was routinely subjected to SEM/XRD to check for the distribution of the prevalent Bravais lattices; some basic unit cells are depicted in Figure 17.

Again, the preferrable and utmost reliable target is the 1,1,1 configuration as shown in Figure 13. Typically on annealing copper at elevated temperatures (e.g., 150°C, 2 hr.), the proportions of the monitored lattices may substantially change, and the degree of the latter does also impact the overall copper performan-

Figure 16: PCB via fill and TH plating.

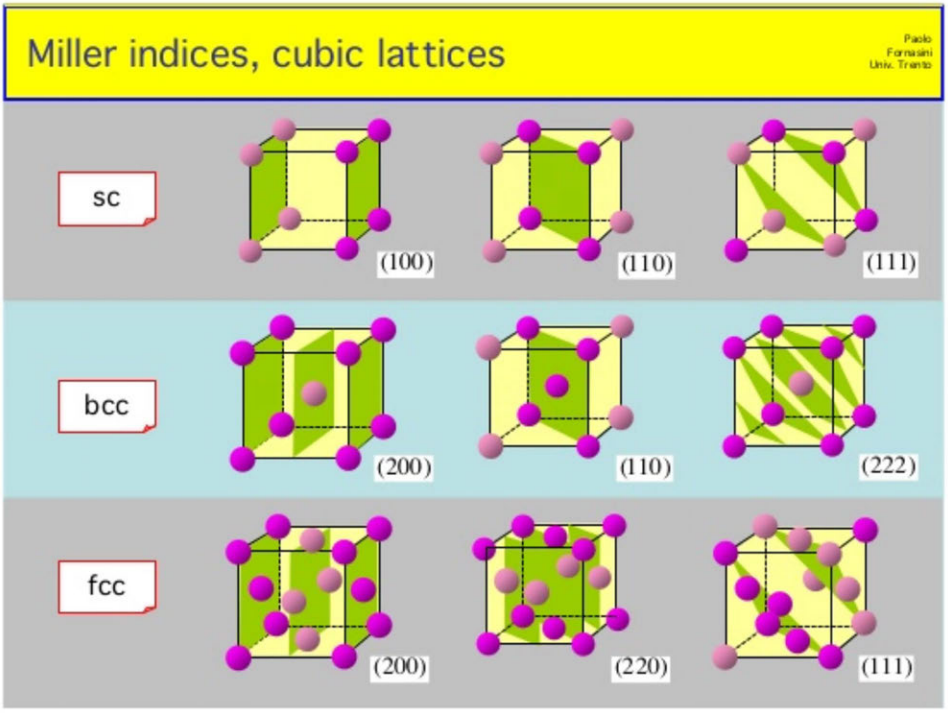


Figure 17: Basic metal lattices.

Various data	Lit. Value Cu	Fill Cu	Fill Cu annealed
111	100	100	100
200	46	39.5	35.4
220	20	17.6	15.2
311	17	6.4	7.9
Lattice constant a [Å]	3.615	3.613	3.612
Density [g/cm³]	8.92	8.948	8.959
Stress [Mpa]	----	-5.5 ± 3.2	1.9 ± 3.1

Table 6: Copper crystallography of a VF-TH copper plating bath (relative intensities in %).

ce. Shown in Table 6 are the achievable crystal data of a viafill (VF) and through-hole (TH) electrolytic copper plating bath.

Perfect 1,1,1 unit cells being grown to flawless copper grains and subsequent void-free crystallites are shown in Figure 18, a SEM of an ion-milled (FIB) copper layer being subsequently subjected to X-ray diffraction (XRD) for the above mentioned copper crystal data aquisition. This configuration does not tend to undergo the vacancy-copper flux Kirkendall mechanism.

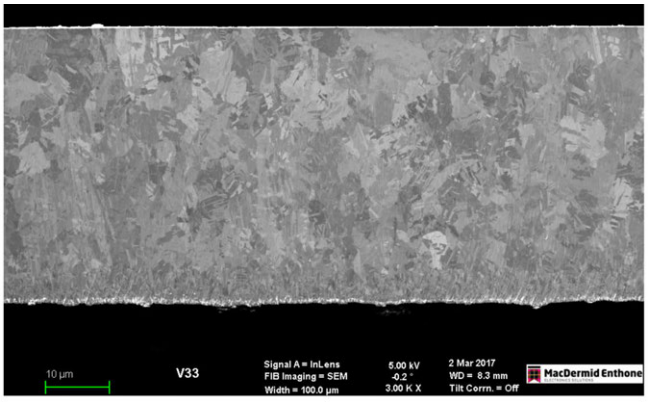


Figure 18: Perfect and void-free VF-TH copper crystallization.

tracqms

THE RIGHT APPROACH CONSULTING LLC

Now is the perfect time for you to take the right approach to quality management.

The single best improvement you can make to your business is to update your QMS. I can help you upgrade to ISO 9001: 2015 or AS9100 Rev D in six months - guaranteed!

LEARN MORE ABOUT MY CERTIFICATION GUARANTEE

tracqms.com

Conclusion

The Macro PCB Section: Extreme Pillars at Work

An impression of the overall challenges of pillar plating is shown in Figure 19. Seeing it from a bird´s eye view, it takes all disciplines to achieve the desired copper plating performance providing seamless electrical and thermal paths, from die to environment, including:

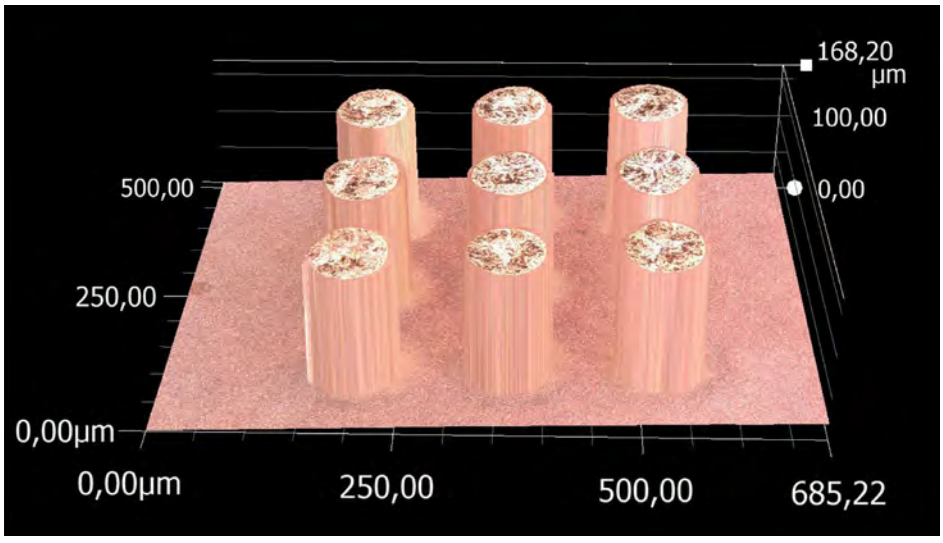


Figure 19: Impression of pillar plating works.

- Additives design
- E-chemistry
- Hydrodynamics
- Equipment/CD regime

This article was originally presented at SMTA International 2017 in Rosemont, Illinois and published in the proceedings.

References

1. "Eliminate Kirkendall Voids in Solder Reactions on Nanotwinned Copper," Tao-Chi Liu et al., *Scripta Materialia* 68 (2013) 241-244.

2. "Failure Mechanisms of Solder Interconnects Under Current Stressing in Advanced Electronic Packages," Y.C. Chan et al., *Progress in Materials Science* 55 (2010) 428-475.

3. "Aging Studies of Cu-Sn Intermetallic Compounds in Annealed Surface Mount Solder Joints," Alex C. K. So et al., *IEEE Transactions on Components, Packaging, and Manufacturing Technology*–Part B, Vol. 20, No. 2, May 1997.

4. "Investigation of Diffusion and Electromigration Parameters for Cu-Sn Intermetallic Compounds in Pb-free Solders Using Simulated Annealing," Brook Chao et al., *Acta Materialia* 55 (2007) 2805-2814.

5. "Formation and behavior of Kirkendall voids within intermetallic layers of solder joints," Doosoo Kim et al., *J Mater Sci: Mater Electron* (2011) 22:703-716.

6. "Role of Kirkendall Effect in Diffusion Processes in Solids," C. A. C. Sequeira et al., Trans. Nonferrous Met. Soc. China 24(2014) 1-11.

7. "Copper Plating Process for Filling Microvias and Through-holes with Minimum Surface Deposition," Maria Nikolova et al., EIPC Summer Conference, Luxemburg (2013) *Conference Proceedings*.

8. "Electroplated Copper Filling of Through-holes: Influence on Hole Geometry," Ron Blake et.al., *The PCB Magazine*, Jan (2017).

Albert Angstenberger is global technical manager, Metallization, MacDermid Enthone Electronic Solutions.

Eric Walch is R&D chemist, MacDermid Enthone Electronic Solutions.

Christian Rietmann is senior R&D chemist, MacDermid Enthone Electronic Solutions.

“Mark does an outstanding job detailing what needs to be included in the handoff from designer to fabricator. This book should be required reading for every designer.

Douglas Brooks, Ph.D.
BS/MS EE

Most of the design data packages that a fabricator receives contain inaccurate or incomplete data.

Don't be a data violator!

DOWNLOAD NOW

I-007e Books

I-007eBooks.com/data

MilAero007 Highlights

IPC Lauds Government Act to Advance Workforce Education ▶

IPC—Association Connecting Electronics Industries is applauding the U.S. Congress for sending legislation to President Trump that will strengthen workforce education and training efforts.

Trump to Sign Defense Electronics Legislation ▶

U.S. President Donald Trump is expected to sign legislation that will bring greater focus and long-term leadership to the government's interests in military electronics.

George Janosko Joins Ventec International Group Technical Sales Team for Midwest USA ▶

Ventec International Group Co., Ltd., a world leader in the production of polyimide and high-reliability epoxy laminates and prepregs, announced the appointment of George Janosko, responsible for technical sales for the U.S. Midwest.

IMPACT on DIVSYS and NWSC Crane ▶

I-Connect007's Patty Goldman has known DIVSYS' Stan Bentley for many years, having met when the company was called Diversified Systems and they made circuit boards and finished products at their facility in Indianapolis. They saw each other at IMPACT recently, and of course had to have a chat.

A Surprising Agreement Between the EU and U.S. on Transatlantic Trade ▶

On July 25, EU Commission President Jean-Claude Juncker and U.S. President Donald Trump struck an agreement on transatlantic trade during President Juncker's visit to Washington D.C. Both parties agreed to work together on a reform of the WTO to address unfair trading practices.

Utility Drones Market to Reach $538.6 Million by 2023

The global utility drones market is expected to grow from an estimated $110.2 million in 2018 to $538.6 million by 2023, at a CAGR of 37.34% from 2018 to 2023. ▶

Eltek Receives Non-Compliance Notice from Nasdaq ▶

Eltek Ltd. received a notice from Nasdaq advising that in light of the resignation of Lian Goldstein, an independent director, the company is currently not in compliance with Nasdaq's audit committee requirements as set forth in the Nasdaq Listing Rules.

Calumet Electronics on IMPACT 2018 ▶

This year at IMPACT Washington, D.C., I-Connect007's Patty Goldman sat down with Steve Vairo and Mike Kadlec of Calumet Electronics, to get their overview on the event.

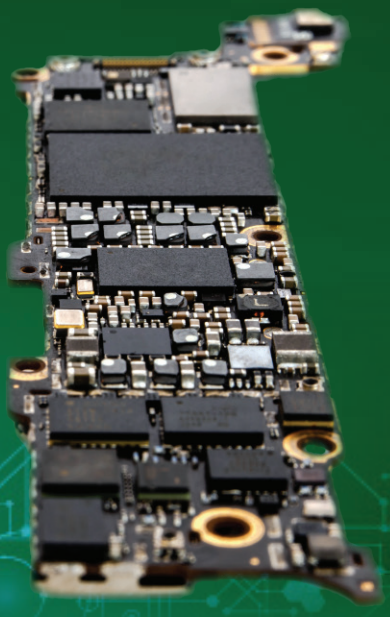
Rockwell Collins and Lockheed Martin to Present a Dual Keynote at SMTA International 2018 ▶

The SMTA is pleased to announce Ron Heberlein, Rockwell Collins, and Tony "Brick" Wilson, Lockheed Martin, will keynote SMTA International the morning of Tuesday, October 16 with their presentation "The World's Most Advanced Fighter Jet Helmet—from Development and Production to the Fight."

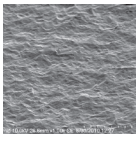
Army's New 3-D Printed Shape-Shifting Soft Robots Crawl, Jump, Grab ▶

New 3-D printed robotic structures can squeeze in tight spaces like a crack in the wall of a cave, jump over trip wire or crawl under a vehicle—all complex Army-relevant functions impossible for humans to perform safely.

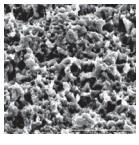
WONDERING HOW TO GET STARTED WITH MSAP?



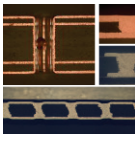
Get with the industry leader - **MacDermid Enthone.** We have the know-how and expertise to bring your manufacturing process to the next level for today's advanced consumer electronics.



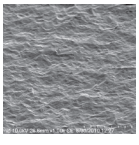
COPPER REDUCTION
CIRCUETCH 100



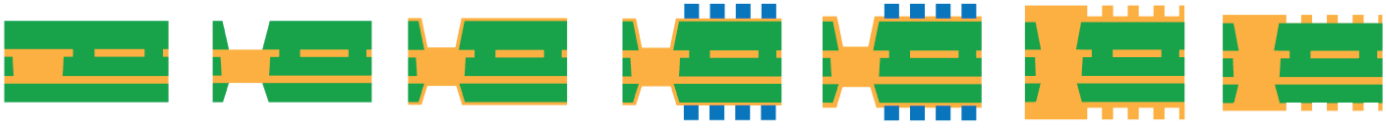
DRY FILM ADHESION
MULTIPREP 200

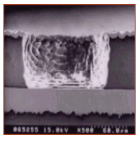


SECONDARY METALLIZATION
MACUSPEC VF-TH

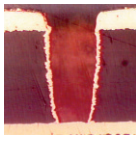


DIFFERENTIAL ETCH
CIRCUETCH 200

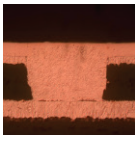




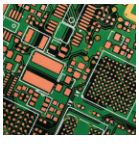
INNERLAYER ADHESION/
LDD PRETREATMENT
MULTIBOND 500



PRIMARY METALLIZATION
SHADOW LE



ADVANCED VIA FILL
MACUSPEC AVF 700



FINAL FINISHES
AFFINITY, ENTEK PLUS HT

MacDermid Enthone
ELECTRONICS SOLUTIONS

227 Freight Street, Waterbury, CT 06702 USA

For more information:
electronics.macdermidenthone.com
infoelectronics@macdermidenthone.com

Global Sourcing: The 5 Cs of Choosing the Right PCB Supplier

The Right Approach
by Steve Williams, THE RIGHT APPROACH CONSULTING

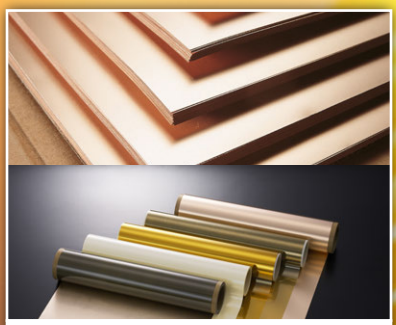
Global sourcing is a complex process and choosing a supplier is always an important decision. The higher the technology, the more important the process for choosing the right one. Considering the highly complicated process of manufacturing printed circuit boards, these guidelines will assist in your decision.

1. Communication

Establishing an open line of communication with any supplier is certainly important, but when working with a PCB manufacturer, it becomes mission critical. Effective two-way communication is at the heart of any strong business relationship. If you don't talk to your suppliers, you won't learn enough about them to build these relationships. Looking at all the various commodities within the electronics industry, the one with the most opportunities for failure is PCBs. Early engagement between the PCB fabricator and customer is critical during the initial stages of a new product launch. Technical questions are always part of the communication process and a breakdown at this stage will create delays and put product reliability at risk. Accessibility to a direct line of communication between both sides will avoid these concerns. However, this communication does not stop at the engineering door; it must continue throughout the PCB manufacturing process. A supplier that provides real-time order updates will minimize the impact to the

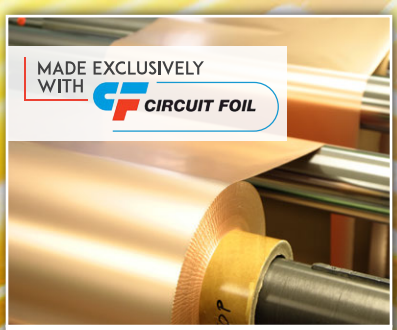
MATRIX
CIRCUIT BOARD MATERIALS

The Gold Standard in PCB Materials and Services



Panasonic

Multilayer & Flex Laminates

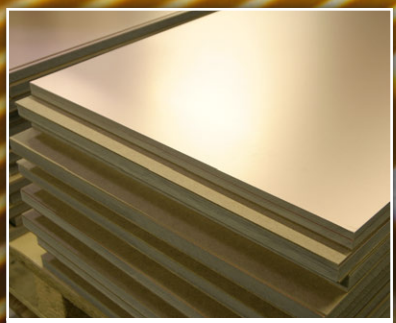


ADVANCED COPPER FOIL

High Quality ED Copper Foils

JINZHOU

Drills, Routers & Endmills



KB
KINGBOARD

Rigid CCL

Hakuto

Film Laminators

AE ADVANCED ENGINEERING

Panel Handling Automation

1-800-668-5447 • www.matrixusa.us

TORONTO • SANTA ANA • SANTA CLARA • CHICAGO • MINNESOTA

customer. Keep in mind that the equation gets more complicated when working with an offshore supplier because the communication channel must bridge time-zone and language challenges.

2. Collaboration

Before selecting a global PCB supplier, it's important to understand if the company has the internal capability and strategy alignment to make the relationship a success. Under-investing in this due diligence is one of the top reasons supplier collaborations fail. The right supplier needs to have the capability to meet the customers' current technological needs, and the ability to anticipate and develop additional technology to meet future needs. One benefit of strong supplier/customer collaboration is the understanding of what the PCBs supplied will be used for and what causes problems in the final product. Going back to the earlier point of communication, another key benefit of collaboration is the reduction of quality issues due to early design engagement. Perhaps the most important benefit of collaboration for the customer is cost reduction. Design for manufacturability (DFM), alternate material suggestions, and minimizing over-engineered designs will result in hard savings and avoided delivery delays.

3. Credibility

PCB manufacturing is engineering intensive and requires operational process excellence. One thing to look for is strong engineering expertise and a solid industry reputation for product quality in the technology you are going to be placing with the supplier. A proven track record on delivery, quality, and flexibility are good starting points. Looking at who else they do business with is another strong indicator of the supplier's credibility. Other customers in the same market sector as you will provide confidence that the supplier understands the intricacies and idiosyncrasies of your business and meets them on a daily basis. Credibility is all about building trust, and trust with your supplier relationships is crucial for achieving supply chain excellence. Another aspect of credibility is whether the supplier is authentic; in other words, do they do what they say? When your PCB supplier give you a delivery date, you need to be highly confident that they are going to meet it. The same confidence must also apply to product quality; and since PCBs are the backbone of any electronic product, failure is not an option.

4. Complete PCB Solution

When choosing a global PCB supplier, it is infinitely more beneficial to select a supplier that can build as much of your technological requirements as possible. In the world of PCB sourcing, not following this model can quickly result in an explosion in the number of suppliers you will need and have to manage. While no supplier is a one-stop shop, minimizing the number of suppliers in your supply base will also minimize your supply chain costs. Technology, surface finish, layer count, and substrate materials are some of the variables that must be considered when assessing a potential PCB supplier's capability. In addition, product-type capability must be evaluated, such as rigid, rigid-flex, radio-frequency (RF), and metal core PCBs. Covering all of your requirements with the fewest suppliers will pay dividends in both qualification costs and the cost of ongoing supplier management.

5. Continuity

One of the biggest supply-chain risks is continuity of supply, and working with a supplier on another continent adds a multitude of logistical challenges to the mix. This is listed last because the previous four considerations can all impact supply continuity. Poor communication can result in delivery delays due to process issues or miscommunications. Finding out in mid-production that a supplier can't build a particular part results from a lack of collaboration. A supplier that frequently reschedules promised delivery dates does not have the needed credibility to avoid supply disruptions. A supplier with below average engineering expertise is not a complete PCB solution. Assuming these four aspects are covered, there are some other things that can

be done to minimize supply disruption. One thing to look for is a supplier that has multiple facilities so that if one is subject to a natural disaster, for example, your product can be temporarily moved to another plant. In some regions of the world, having an independent source of electricity is another critical factor to avoid supply delays. Finally, choose a supplier that has a formal business continuity plan in place.

The credibility and reputation of your company is based in part on your supply chain and you are only as good as your weakest link. Choose wisely. **PCB007**

Steve Williams is the president of The Right Approach Consulting. To contact Williams, or read past columns or contact williams, click here.

Texas Engineers Work with Uber and Army Research Labs on uberAIR

Researchers in the Cockrell School of Engineering at The University of Texas at Austin will work with the U.S. Army Research Labs (ARL) and Uber Elevate to help develop new rotor technology for vehicles to be used in Uber's proposed urban aviation ride-share network—uberAIR.

Last year, Uber announced that the first Uber Elevate cities would be Dallas (DFW metroplex) and Los Angeles, with a goal of flight demonstrations in 2020 and plans to make uberAIR commercially available to riders in those cities by 2023. As part of the uberAIR program, the company has entered into partnerships with several major aircraft manufacturers and signed a space act agreement with NASA, which will stimulate the development of new unmanned traffic management concepts and aerial safety systems.

The design of the vertical take-off and landing (VTOL) aircraft to be used in the project specifies that it is a fully electric vehicle with a cruising speed of 150-200 mph, a cruising altitude of 1,000-2,000 feet and the ability to complete trips of up to 60 miles on a single charge.

"UT is uniquely positioned to contribute to this new technology," said Jayant Sirohi, associate professor in UT's Department of Aerospace Engineering and Engineering Mechanics and the UT team leader on the project. "In addition to the technical expertise we bring to this area, we also already have a rig to test new rotor configurations right here on campus."

Sirohi is one of the country's leading experts in unmanned aerial vehicle (UAV) technology, VTOL aircraft and fixed- and rotary-wing aeroelasticity. He and his team, which includes postdoctoral fellow Christopher Cameron and Charles Tinney from UT's Applied Research Laboratories, will explore the efficiency and noise signature of stacked co-rotating rotors, or propellers, for VTOL.

(Source: The University of Texas at Austin)

Meet Nicolas Robin, IPC's New Senior Director in Europe

One World, One Industry

by John Mitchell, IPC–Association Connecting Electronics Industries

In May, IPC Europe welcomed new Senior Director Nicolas Robin. Based in Brussels, Nicolas will represent IPC and the electronics manufacturing industry in Europe. I recently sat down with Nicolas for a one-to-one conversation to get to know him better and introduce him to fellow electronics industry members.

John Mitchell: Nicolas, as senior director in Europe, what do your responsibilities include?

Nicolas Robin: In this role, I serve as IPC's representative before European governmental officials, institutions, and public policy stakeholders. I will also be the coordinator and operational point of contact for IPC's European membership.

Mitchell: Where did you work prior to IPC?

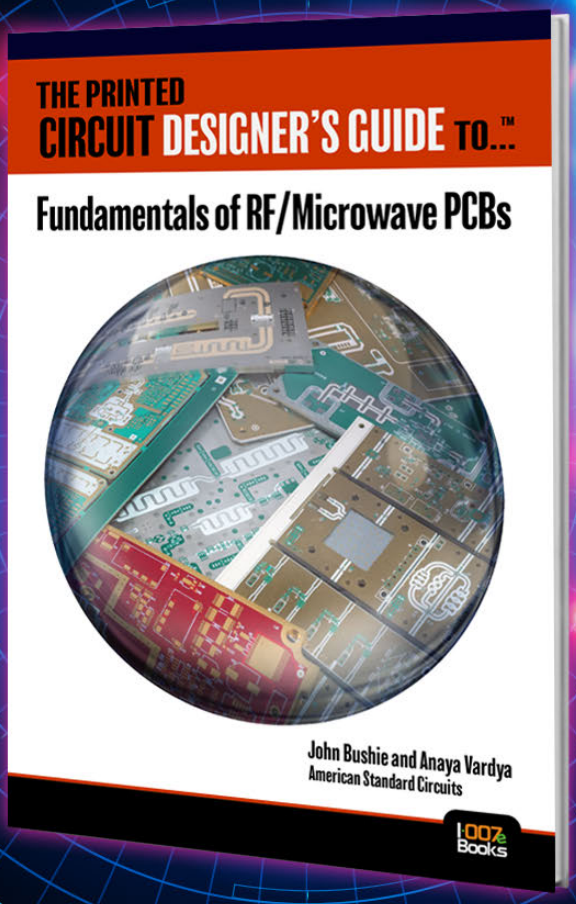
Robin: Prior to this position, I was public affairs director for the world's largest glass container company—Owens-Illinois (O-I). I represented O-I in government affairs at the European Union and throughout Europe. I also worked with the European sustainability program leadership in support of corporate sustainability goals, including increasing the company's use of recycled content. I have more than 25 years of experience in advocacy for companies at the European Union and national levels. I was director of public affairs for various consulting firms and assistant to a French member of the European Parliament. As a research fellow at Johns Hopkins University (USA), I conducted a series of seminars on European integration and its economic impact.

Mitchell: What are your goals for IPC Europe?

Robin: Currently, our European membership represents more than 600 sites. A new dynamic has been engaged in the region. Therefore, my goal is to expand IPC's brand in Europe, reinforce IPC's presence at a national level, and provide a full member and customer satisfaction service. To reach these objectives, IPC Europe will continue developing local activities for the industry, including networking and exchange of experience opportunities. We are running approximately 20 events across Europe in 2018. We want to strengthen our programs for specific segments of importance for our industry, such as automotive or medical devices. We will continue to support IPC education programs and IPC Europe's network of training centers. I would like to facilitate European industry participation in IPC activities, especially standards development.

Regarding public affairs, my objective is to increase IPC's value for members as a source of policy information and advocacy, and ultimately make IPC a principal advocacy platform for our members. To this end, we are going to launch IPC's European Government Relations Committee composed of the members who would like to engage in shaping our positions on policy issues affecting the industry.

Designers, get this book on your radar, now!



Today's designers are challenged more than ever with the task of finding the optimal balance between cost and performance when designing radio frequency/microwave PCBs. This book gives a better understanding of the issues related to the design and manufacture of FR/microwave devices from the perspecitve of the PCB fabricator.

I-007e Books

Download Now

I am encouraged by the first responses I have received from our members who want to join this committee. We also plan to organize a series of webinars to provide members with increased value-added information, services, and opportunities, such as engaging directly with policymakers.

Mitchell: What are the biggest concerns you've noticed among IPC Europe's members? What has IPC been doing to address those concerns?

Robin: My exchanges with our members indicate that a major concern for the European industry is a skilled workforce shortage. Many members have experienced difficulties recruiting skilled employees and attracting young people. IPC fills the needs of its members in this area through its network of training centers and online training opportunities. The recently launched Job Tasks Analysis Committee will pave the way for a new competency model for the electronics industry. We are bringing these initiatives to the attention of policymakers and encouraging them to promote vocational training and lifelong learning, which are keys to re-educating workers to fill the jobs IPC continues to create.

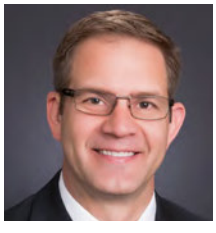
IPC members are also concerned by overly burdensome environment and chemical regulations. The substitution of substances of concern is a long and cost-intensive process with little certainty that the developed alternatives will not be restricted after a certain period. IPC advocates for smart and proportionate environmental regulations that ensure the right balance between risks, costs, and benefits. The European Commission is currently looking at the issue of interface between chemical, product, and waste legislation. This could potentially result in the introduction of new requirements for the design of products and the tracking of substances of concern throughout the supply chain. As an association representing all facets of the electronics industry, IPC clearly has a role to play here. Moreover, the recent decision by the European Chemicals Agency to include lead metal on the list of Substances of Very High Concern (SVHC) will have significant consequences for IPC members in Europe. IPC will engage in an advocacy and communication campaign in partnership with the International Lead Association on this issue.

Mitchell: Is there anything new or different that you'd like to share about this year's IMPACT Europe?

Robin: IMPACT Europe 2018 will be in Brussels, Belgium, November 28–29. It will focus on some of the most pressing challenges for our industry. We will kick off the event with a policymakers dinner, followed by a full day of sessions on topics such as conflict minerals, chemical legislation, and the interface between chemical and waste legislation. One of the novelties this year will be a public event on skills and workforce needs featuring high-level speakers from EU institutions and the industry. We will also bring IPC members to meet with Members of the European Parliaments (MEPs) and learn more about their priorities ahead of the 2019 European elections. Our discussion will lead to a declaration of IPC's priorities for the next policy cycle and urge policymakers to ensure an appropriate regulatory environment for a thriving electronics industry in Europe.

Mitchell: To wrap up, Nicolas, what do you like to do in your spare time?

Robin: I grew up in the coastal port city of Marseille, France. Thus, I love to swim and participate in all kinds of nautical sports. Since my teens, I have been involved in French and European politics both as an actor and observer of the often complicated and Byzantine world of how Brussels functions. Married to an Egyptologist, I am also interested in ancient Middle Eastern civilizations. **PCB007**



John Mitchell is president and CEO of IPC–Association Connecting Electronics Industries. To read past columns or contact Mitchell, click here.

Why Choose Fein-Line?

Because there is a Fine Line between winning and the alternative.

Fein-Line Associates is a consulting group serving the global interconnect and EMS industries, as well as those needing contact with/information regarding the manufacture and assembly of Printed Circuit Boards. The principal of Fein-Line Associates, Dan (Baer) Feinberg, formally president of Morton Electronic Materials (Dynachem) is a 50+ year veteran of the printed circuit and electronic materials industries. Dan is a member of the IPC Hall of Fame; has authored over 150 columns, articles, interviews, and features that have appeared in a variety of magazines; and has spoken at numerous industry events. He covers major events, trade shows, and technology introductions and trends.

Mr. Feinberg and his associates specialize in:

- management consulting
- technology transfer
- new product market entry
- merger and acquisition due diligence
- market information and market research
- expert witness assistance and seminars regarding all aspects of printed circuits
- electronic assembly manufacturing and marketing

Dan (Baer) Feinberg

Fein-Line Associates, Inc.
P.O. Box 73355
San Clemente, CA 92673

Telephone: (949) 498-7866
Email: baer@feinline.com

Fein-Line ASSOCIATES, INC.

www.feinline.com

Recent Highlights from PCB007

1 Industry Veteran Nolan Johnson Joins I-Connect007 Editorial Team ▸

I-Connect007 welcomes the recent addition of industry veteran Nolan Johnson to its editorial team. In his new position, Johnson will take over as managing editor of *SMT007 Magazine* and *PCB007 Magazine*. Nolan brings 30 years of career experience focused almost entirely on electronics design and manufacturing.

2 An Owner's Positive Take on IMPACT 2018: American Standard Circuits' Founder & Chairman Gordhan Patel ▸

During a full day at IMPACT 2018, I had a chance to speak with American Standard Circuits' founder and chairman Gordhan Patel. We had much to talk about after listening to several speakers from the departments of Defense and Education, and the International Trade Administration.

3 The PCB Norsemen: Lean Challenges–Standard vs. Non-Standard Products ▸

Writes Didrick Bech: People tend to treat standard and non-standard products in the same way; however, they represent two parallel product segments and consequently different challenges for your Lean manufacturing process, especially in relation to production and logistical operations. When you fail to differentiate the processing of standard and non-standard products, not only is the Lean manufacturing process disrupted, but you also introduce a variety of production, financial and logistical challenges.

4 Welcome to the Silicon Valley Neighborhood: Nano Dimension Arrives in California ▸

I-Connect007 Technical Editor Dan Feinberg accepted an invitation recently to tour Nano Dimension's new USA headquarters in Santa Clara's Silicon Valley, which included a sit-down with President and Co-Founder Simon Fried.

5 Graphic PLC Team Completes Business Improvement Apprenticeship ▸

The 12-month program is a formally recognized NVQ apprenticeship qualification combining classroom-based learning and simulations alongside practical improvement projects, providing an opportunity to apply the skills they have gained.

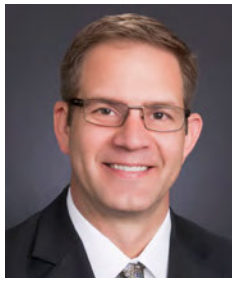
6 DSBJ Completes Acquisition of Multek ▸

Multek announced the completion of its previously announced acquisition by Suzhou Dongshan Precision Manufacturing Co. Ltd., a diversified manufacturer headquartered in Suzhou, China.

7 It's Only Common Sense: A Peek at Future Technological Advancements ▸

It's that time again—time for a peek into the future. The following ideas come from an excellent book by Mark Penn called Microtrends Squared: The New Small Forces Driving Today's Big Disruptions.

8 One World, One Industry: Automotive Electronics–Past/Present/Future ▸



As electronics play an increasingly important role in automotive manufacturing, tremendous change and great progress have been made worldwide. We are at the crossroads of incredible technological advancements, and it's been exhilarating to watch. I am eager to see what happens next.

9 Cirexx Supplies Rigid-Flex Circuits for Innovative Medical Application ▸

The material toolbox idea first came up when I saw the IPC appendix list for standard one-ply stack-ups. The idea is to make a very simple bill of materials, specifications and notes, and possibly use the same prepreg/resin in the laminate and in the core.

10 North American PCB Industry Growth Trend Continues in June 2018 ▸

IPC—Association Connecting Electronics Industries announced today the June 2018 findings from its North American printed circuit board (PCB) Statistical Program. Industry shipments and orders in June continued to grow at a strong pace. The book-to-bill ratio for June is 1.05.

Career Opportunities

Pssst! Are You Looking for Someone?

Place your notice in our Help Wanted section.

For just $500, your 200 word, full-column—or, for $250, your 100 word, half-column—ad will appear in the Help Wanted section of all three of our monthly magazines, reaching circuit board designers, fabricators, assemblers, OEMs and suppliers.

Potential candidates can click on your ad and submit a résumé directly to the email address you've provided. If you wish to continue beyond the first month, the price is the same per month. No contract required. We even include your logo in the ad, which is great branding!

To get your ad into the next issue, contact:
Barb Hockaday at barb@iconnect007.com or +1.916.608.0660 (-7 GMT)

I-Connect007
GOOD FOR THE INDUSTRY

smt007 pcb007 pcb design007

Career Opportunities

ELECTROLUBE
THE SOLUTIONS PEOPLE

Sales Development Manager

Electrolube has a new opportunity for a sales development manager covering the Midwest United States. This is an exciting role involving all aspects of sales development and account management for the Electrolube brand.

The successful candidate will have relevant experience within the electro-chemicals industry and a strong commercial background. This position will report directly to the U.S. general manager.

Applicants should apply in writing and submit a CV by clicking the button below.

apply now

Ucamco
Former Barco ETS

International Field Service Engineer located in ITALY

The successful candidate will:

- Install and service our plotters and direct imaging machines at customer sites Europe-wide
- Carry out maintenance in the field
- Frequent travel: 4 to 5 days a week, 3 to 4 weeks a month
- Assist product manager

We are looking for a team player who is:

- Strongly customer-oriented and experienced in on-site support
- Accustomed to travel, and willing to travel frequently
- Motivated, independent and enterprising
- Technically-minded with training/background in electromechanics/electronics
- Experienced with software (setup, configuration, and usage of Windows-based CAM front-end software and Linux-based RIP software)
- Fluent in Italian and English (German and/or French is a plus)
- An analytical thinker
- Capable of problem solving

The right candidate will be a valued member of a friendly, team-oriented, growing international company that is a leader in its field, dedicated to excellence in all it does. Dynamic and fun, the company offers a great working atmosphere, and this new position is forward-looking and open, with plenty of opportunities for enterprising individuals whose results could be rewarded with prospects for progression in technical development.

Apply to Anja Ingels after clicking below.

apply now

Career Opportunities

MacDermid Enthone
ELECTRONICS SOLUTIONS

Product Group Field Manager
Waterbury, CT

Do you have what it takes? MacDermid Enthone Electronics Solutions is a leading supplier of specialty chemicals, providing application-specific solutions and unsurpassed technical support.

The position of the Product Group Field Manager will be responsible for creating and driving a strategic plan for the regional product line, including the following:

- Possess a thorough understanding of the overall PCB business, and specifics in wet processing areas
- Play an integral part in developing a commercial and technical customer strategy
- Create and deliver customer facing presentations
- Provide technical training for field staff
- Create and execute a product rationalization program
- Develop new product roll-out packages

Hiring Profile

- Bachelor's degree or 5 years' job-related experience
- Strong understanding of chemistry and chemical interaction within PCB manufacturing
- Excellent written and oral communication skills
- Strong track record of navigating technically through complex organizations
- Willingness to travel

apply now

GO Gardien

Role: Vice President Gardien Taiwan
TAOYUAN COUNTY, TAIWAN

Gardien Taiwan is a service provider of circuit board (PCB) quality solutions, including electrical testing, AOI optical inspection, engineering (CAM), fixture making, repair and rework. Gardien Taiwan operates service centers in Taoyuan and employs about 100 employees and is currently seeking a vice president to manage and oversee the entity.

Candidate Profile:

- Proficiency in Chinese and English (written and spoken)
- Excellent communication and organization skills
- Experience in change management
- PCB background appreciated, but not mandatory
- Management experience in internationally operating companies
- Savvy in standard office software (Word, Excel and Power Point)

If this sounds like you, please click here to send us an email with your attached CV.

About Gardien Group - Gardien is the world's largest international provider of independent testing and QA solutions to the PCB industry with a global footprint across 24 service centres in five countries and we cater to a whole range of customers, from small family owned PCB shops to large international fabricators. Gardien's quality solutions and process standards are trusted by leading high-tech manufacturers and important industries including aerospace, defense, and medical technology.

apply now

Career Opportunities

ZENTECH

Zentech Manufacturing:
Hiring Multiple Positions

Are you looking to excel in your career and grow professionally in a thriving business? Zentech, established in Baltimore, Maryland, in 1998, has proven to be one of the premier electronics contract manufacturers in the U.S.

Zentech is rapidly growing and seeking to add Manufacturing Engineers, Program Managers, and Sr. Test Technicians. Offering an excellent benefit package including health/dental insurance and an employer-matched 401k program, Zentech holds the ultimate set of certifications relating to the manufacture of mission-critical printed circuit card assemblies, including: ISO:9001, AS9100, DD2345, and ISO 13485.

Zentech is an IPC Trusted Source QML and ITAR registered. U.S. citizens only need apply.

Please email resume below.

apply now

Manncorp™

Sales Associate - Mexico

Manncorp, a leader in the electronics assembly industry for over 50 years, is looking for an additional sales associate to cover all of Mexico and to be part of a collaborative, tight-knit team. We offer on-the-job training and years of industry experience in order to set up our sales associate for success. This individual will be a key part of the sales cycle and be heavily involved with the customers and the sales manager.

Job responsibilities:
- Acquire new customers by reaching out to leads
- Ascertain customer's purchase needs
- Assist in resolving customer complaints and queries
- Meet deadlines and financial goal minimums
- Make recommendations to the customer
- Maintain documentation of customer communication, contact and account updates

Job requirements:
- Located in Mexico
- Knowledge of pick-and-place and electronics assembly in general
- 3+ years of sales experience
- Customer service skills
- Positive attitude
- Self-starter with ability to work with little supervision
- Phone, email, and chat communication skills
- Persuasion, negotiation, and closing skills

We offer:
- Competitive salary
- Generous commission structure

apply now

Career Opportunities

Mentor®
A Siemens Business

PCB Manufacturing, Marketing Engineer

Use your knowledge of PCB assembly and process engineering to promote Mentor's Valor digital manufacturing solutions via industry articles, industry events, blogs, and relevant social networking sites. The Valor division is seeking a seasoned professional who has operated within the PCB manufacturing industry to be a leading voice in advocating our solutions through a variety of marketing platforms including digital, media, trade show, conferences, and forums.

The successful candidate is expected to have solid experience within the PCB assembly industry and the ability to represent the Valor solutions with authority and credibility. A solid background in PCB Process Engineering or Quality management to leverage in day-to-day activities is preferred. The candidate should be a good "storyteller" who can develop relatable content in an interesting and compelling manner, and who is comfortable in presenting in public as well as engaging in on-line forums; should have solid experience with professional social platforms such as LinkedIn.

Success will be measured quantitatively in terms of number of interactions, increase in digital engagements, measurement of sentiment, article placements, presentations delivered. Qualitatively, success will be measured by feedback from colleagues and relevant industry players.

This is an excellent opportunity for an industry professional who has a passion for marketing and public presentation.

Location flexible: Israel, UK or US

apply now

BLACKFOX
Premier Training & Certification

IPC Master Instructor

This position is responsible for IPC and skill-based instruction and certification at the training center as well as training events as assigned by company's sales/operations VP. This position may be part-time, full-time, and/or an independent contractor, depending upon the demand and the individual's situation. Must have the ability to work with little or no supervision and make appropriate and professional decisions. Candidate must have the ability to collaborate with the client managers to continually enhance the training program. Position is responsible for validating the program value and its overall success. Candidate will be trained/certified and recognized by IPC as a Master Instructor. Position requires the input and management of the training records. Will require some travel to client's facilities and other training centers.

For more information, click below.

apply now

Career Opportunities

Mentor®
A Siemens Business

Technology Communications Writer/Content Manager
Board Systems Division

Mentor Graphics, a Siemens business, is a global technology leader in EDA software, enabling global companies to develop new and highly innovative electronic products in the increasingly complex world of chip, board, and system design.

Job Duties:

The Mentor printed circuit board (PCB) technical writer/content manager will:

- Write and produce high-quality content for various properties (blogs, product collateral, technical white papers, case studies, industry publications, etc.)
- Gather research and data, interview subject matter experts, and transform complex information into clear, concise marketing communications
- Manage projects across multiple PCB product teams (high-speed design/analysis, advanced packaging, board design) within a deadline-driven environment

Job Qualifications:

The ideal candidate should possess:

- Strong writing and editing skills with experience in PCB design technologies
- Desktop publishing skills (InDesign) using project templates and knowledge of online publications and social media
- A technical background (B.S. in electrical engineering or computer science preferred; this role works closely with the PCB division's technical marketing engineers and managers
- Solid project planning and management skills; appreciation for adhering to deadlines; creativity for turning technical information into compelling content; teamwork and strong interpersonal communications skills; ability to be a self-starter

apply now

American Standard Circuits
Creative Innovations In Flex, Digital & Microwave Circuits

CAM Operator

American Standard Circuits is seeking a CAM Operator for its Phoenix, Ariz., office. Qualified applicants will need experience in using Valor/Genesis (GenFlex) CAD/CAM software with printed circuit board process knowledge to edit electronic data in support of customer and production needs.

Job Requirements:

- At least 5 years' experience in PCB manufacturing
- Process DRC / DFMs and distinguish valid design and manufacturing concerns.
- Modify customer supplied data files and interface with customers and engineers
- Responsible for releasing manufacturing tooling to the production floor
- Prepare NC tooling for machine drilling, routing, imaging, solder mask, silkscreen
- Netlist test, optical inspection
- Work with Production on needed changes
- Suggestions on continual improvements for engineering and processing.
- Be able to read write and communicate in English
- Must understand blueprint specifications
- Must be US Citizen or permanent resident (ITAR)
- High School Graduate or equivalent

Join our Team!

Founded in 1988, American Standard Circuits is a leading manufacturer of advanced circuit board solutions worldwide. Our ongoing commitment to leading-edge higher-level interconnect technology, cost-effective manufacturing and unparalleled customer service has put us at the forefront of advanced technology circuit board fabrication.

We manufacture quality rigid, metal-backed and flex printed circuit boards on various types of substrates for many applications.

apply now

Events Calendar

PCB West 2018 ▶
September 11–13, 2018
Santa Clara, California, USA

IPC E-Textiles 2018 Workshop ▶
September 13, 2018
Des Plaines, Illinois, USA

electronica India & productronica India ▶
September 26–28, 2018
Bengaluru, India

electronicAsia 2018 ▶
October 13–16, 2018
Hong Kong

SMTA International ▶
October 16–17, 2018
Rosemont, Illinois, USA

TPCA Show 2018 ▶
October 24–26, 2018
Taipei, Taiwan

electronica 2018 ▶
November 13–16, 2018
Munich, Germany

IDTechEx Show ▶
November 14–15, 2018
Santa Clara, California, USA

IPC IMPACT Europe 2018 ▶
November 28–29, 2018
Brussels, Belgium

HKPCA/IPC International Printed Circuit & South China Fair ▶
December 5–7, 2018
Shenzhen, China

48th NEPCON JAPAN ▶
January 16–18, 2019
Tokyo Big Sight, Tokyo, Japan

IPC APEX EXPO Conference and Exhibition ▶
January 26–31, 2019
San Diego, California, USA

DesignCon 2019 ▶
January 29–31, 2019
Santa Clara, California, USA

Additional Event Calendars

PUBLISHER: **BARRY MATTIES**
barry@iconnect007.com

SALES MANAGER: **BARB HOCKADAY**
(916) 608-0660; barb@iconnect007.com

SALES: **ANGELA ALEXANDER**
(408) 489-8389; angela@iconnect007.com

MARKETING SERVICES: **TOBEY MARSICOVETERE**
(916) 266-9160; tobey@iconnect007.com

MANAGING EDITOR: **PATRICIA GOLDMAN**
(724) 299-8633; patty@iconnect007.com

MANAGING EDITOR: **NOLAN JOHNSON**
(503) 597-8037; nolan@iconnect007.com

TECHNICAL EDITOR: **PETE STARKEY**
+44 (0) 1455 293333; pete@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **DAN FEINBERG**
baer@iconnect007.com

CONTRIBUTING TECHNICAL EDITOR: **HAPPY HOLDEN**
(616) 741-9213; happy@iconnect007.com

PRODUCTION MANAGER: **SHELLY STEIN**
shelly@iconnect007.com

MAGAZINE LAYOUT: **RON MEOGROSSI**

AD DESIGN: **SHELLY STEIN, MIKE RADOGNA , TOBEY MARSICOVETERE**

INNOVATIVE TECHNOLOGY: **BRYSON MATTIES**

COVER: **SHELLY STEIN**

COVER IMAGE: **SHELLY STEIN**

PCB007 MAGAZINE

PCB007 MAGAZINE®
is published by BR Publishing, Inc.,
942 Windemere Dr. NW, Salem, OR 97304

September 2018, Volume 8, Number 9
PCB007 MAGAZINE is published monthly,
by BR Publishing, Inc.

ADVERTISER INDEX

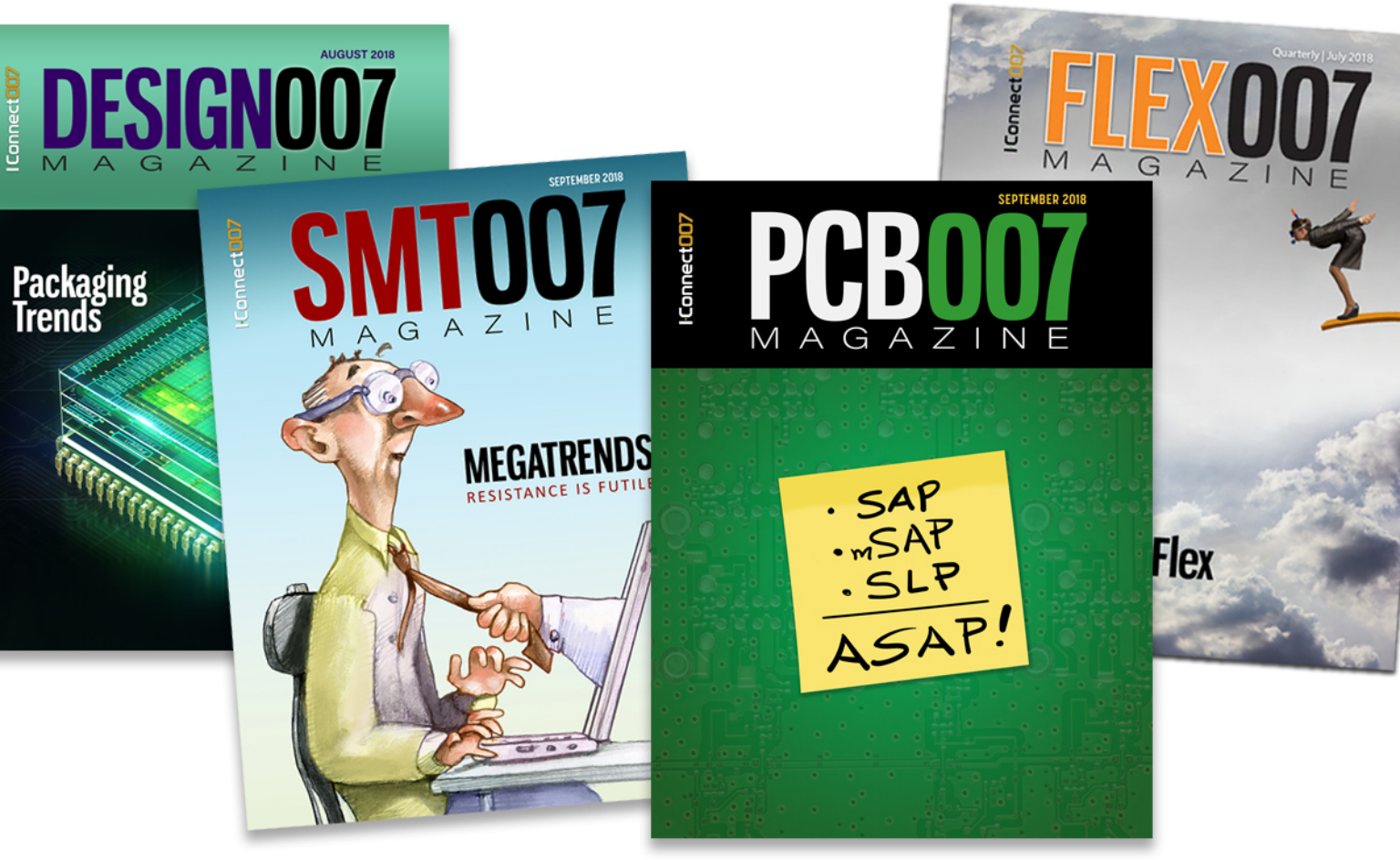
Coming Soon to PCB007 Magazine:

OCTOBER 2018: Lights Out
The Fully Automated Factory

NOVEMBER 2018: Medical Electronics
Opportunities and Challenges

I-Connect007

GOOD FOR THE INDUSTRY



FREE SUBSCRIPTION

myiconnect007.com

mediakit.iconnect007.com

EDITORIAL CONTACT

Patty Goldman

patty@iconnect007.com

+1 724.299.8633 GMT-4

SALES CONTACT

Barb Hockaday

barb@iconnect007.com

+1 916 365-1727 GMT-7

www.iconnect007.com